JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

Analysis of Low-Power CRM's Design and Performance Utilizing CDF

Rajesh Ranjan
M.Tech VLSI
0904EC20MT15
Shriram College of Engineering and Management
Banmore, Gwalior

Prof. Ashish Duvey
Assistant Professor
Shriram College of Engineering and Management
Banmore, Gwalior

Abstract*— The positive attribute of lower power usage has made reversible logic quite popular in recent years. RM (Reversible multiplexers), RDM (reversible de-multiplexers), RE (reversible encoders), and RD (reversible decoders) are among several kinds of combinational circuits used in this design. Researchers and engineers have recently been interested in reversible logic devices and circuits because of their potential applications in fields like digital signal processing, nanotechnology, low-power CMOS, quantum computing, computer graphics, optical computing & encryption. Designing low-power, high-efficiency CDF (COMS DG FINFET) Reversible MUX circuits is difficult. This work explores the internal logic structure and circuit operating of a CMOS Reversible MUX circuit designed using CMOS & CDF components. CDF & CMOS-based CRM (CMOS Reversible MUX) is developed at transistor level. These CRM are simulated employing cadence tool in 90nm technology, and their performance is analyzed contrasting to that of 90nm CDF technology. For greater mobility and transistor scaling compared to other methods, CRM with CDF approaches delivers low leakage current and low leakage power.

Key Words*— CMOS, DG FINFET, CMOS Reversible MUX, Leakage Power, Cadence.

I. INTRODUCTION (HEADING 1)

Reduced silicon space, high throughput hardware, and low power consumption are essential for the growth of mobile operating programs like PDAs and PCs, as well as progress of shrinking technology. [1-3]. Minimal below-threshold Multi-gate transistors, such as double gate FinFETs, are superior to Standard CMOS in terms of swing (SS) and leakage current [4]. Adders are crucial for performing subtraction, multiplication, addition, and division in complex arithmetic circuits. They serve as system's core components and have a big impact on how well DSP-based processors handle tasks like video processing, filtering, and Fast Fourier Transform while using a minimum amount of power and energy. [5-6]. Power consumption is decreased by scaling operating frequency and supply voltage. However, this delay and improvement in driving ability [7-9]. There are several Full Adders that have been invented, and everyone has advantages and disadvantages. Using effective structures, the full adder creates a focal point in carry choose, carry look ahead, carry skip, and conventional adders. [10-11]. Additionally, the Full adder needs to be designed and improved for use at extremely low voltages.

Digital CMOS circuits are often used in computers and other devices that need processing, computation, or analysis of any signal because of their high-speed capabilities. Since CMOS has low noise margins, high performance, and low static power consumption, it is most popular logic family. There is a current and future significant demand for these circuits due to the need for speedier signal processing. An increase in number of incorporated transistors on a processor results in a quicker processing performance for a computer. The increase in energy and power dissipation that comes along with such performance enhancement [12]. Higher energy and power dissipation have drawback of making circuits more expensive to package and need more extensive cooling technology, which lowers reliability and raises costs. A major difficulty in designing high performance circuits is reducing their power and energy consumption, since clock frequency and on-chip integration will keep going up to meet the need for faster processing [13]. TIPS (Tera Instructions per Second) is achieved by using billions of transistors on circuits operating at clock rates surpassing 30 GHz. This speed will increase circuit power usage to thousands of watts. Reliability issues, including thermal stress, hot carrier, and electromigration, are introduced by such a high density of power dissipation and reduce circuit performance. Higher power loss circuits will use more battery energy, necessitating usage of low-power processors and chips which consume less battery energy. [14–16]. For battery-powered portable digital systems such as laptops, notepads, & tablets, the primary concern is minimal power consumption, which also improves battery life.

II. LITERATURE SURVEY

Himanshu Thapliyal and Srinivas[17] recommended TSG gate-based NxN reversible multiplier. In this instance, partial

products are generated in parallel with a delay using Fredkin Gates, and addition operations are simplified into log2N phases using a reversible multiplier that incorporates a TSG gate. Utilizing this reversible multiplier, they have also created 4x4 architecture. Nidhi Pokhriyal et al., [18] suggested an 8x8 Vedic multiplier that uses compressors of ratios 4:3, 5:3, 6:3, and 7:3 to get the total result. By merging the concepts of Vedic sutras Urdhwa Triyakbhyam with modern compression techniques, a powerful but energy-efficient multiplier architecture has been developed. The cadence tool was used for analysis and synthesis of 180 nm technology. Maryam Ehsanpour et al., [19] have created a Modified Full Adder (MFA)-based 4-bit binary multiplier circuit that requires less sophisticated hardware. They've shown that the reversible circuits they've created can function as a reversible full adder, too, and that it needs just a little amount of garbage output and constant input. Madhusmita Mahapatro et al., [20] used reversible logic gates to create arithmetic circuits. Utilizing 0.25-micrometer technology for simulation and synthesis, they have created arithmetic circuits. Full and half adders that can add and subtract in both directions are examples of reversible logic. A 4x4 multiplier circuit and a 4-bit binary parallel adder were created by employing reversible full adders and half adders. Anindita Banerjee and Anirban Pathak [21] Utilising CNT, NOT, and Toffoli (NCT) gates, a reversible multiplier circuit was built. The method relies on a binary tree network to generate all partial products and then put them together. Circuits for producing reversible partial products and for performing parallel addition are developed. This architecture has a low quantum cost, low gate count, and low trash outputs. Jenath and Nagrajan [22] developed a single-precision, floating-point multiplier that can be reversed. Multipliers are created using Peres gates. The multiplier operands are divided into 3 sections, each of eight bits. Nine 8x8 bit multipliers are used to produce a 24x24 bit reversible multiplier. The quantum cost, latency, and trash outputs are all taken into account during construction of an efficient multiplier. VHDL code is used for design, and Xilinx 9.1 simulation tool is used for testing and validation. Kartikeya Bhardwaj and Bharat M Despande [23] presented a Kalgorithm, an enhanced version of Booth's Recoding Algorithm, to simplify hardware required for signed multiplication. An effective multiplier design is also provided for use with this method. Using Booth's Recoding technique, they developed a 4-bit reversible multiplier that is both fault-tolerant and non-fault-tolerant. Using this method, they examined factors like constant inputs, quantum cost, gate count, and garbage values. When contrasted to standard methods, this one reduces the quantum cost by 33 percent. Pradip Panchal et.al, [24] provided some research on utilizing LBP for facial recognition. By segmenting face photos into smaller areas to offer feature information, locally improved LBP is produced. All individual local histograms are combined to create the GLBP image. Face lighting and expression modifications are evaluated to determine how well this approach performs. They have an 80 percent success rate in identifying people using this technique. Bilel Ameur et.al, [25] recommended a project featuring facial recognition. The extraction of features is accomplished by utilising Gabor and LBP wavelets. Utilise the dimension reduction technique to minimise the pattern vector.

III. Implementation and Operation of 2:1 CMOS Reversible MUX Logic

According to this understanding, a quantum computer is a network (or collection of networks) of quantum logic gates, each of which executes a straightforward unitary operation on a single quantum bit (also known as a qubit). Reversible logic gates are non-destructive circuits that may be reversed without losing any data. Their ability to generate distinct output vectors from each input vector and the reverse is a distinguishing feature of reversible logic circuits.

Reversible logic gates are characterised by the fact that the number of inputs and outputs is equivalent, denoted by n = k. Reversibility is conferred upon a gate when the logic of inputs and outputs is identical, and the input vector is recoverable from the output vector independently. Designing reversible logic circuits requires a collection of reversible logic gates. The symbol for an n k reversible logic gate is:

Input Vector

$$I_V = (I_{i,j}, I_{i+2,j}, I_{i+3,j} \dots \dots \dots I_{k-1,}I_{k,j}) \quad (1.1)$$

Output Vector

$$O_V = (O_{i,j}, O_{i+2,j}, O_{i+3,j} \dots \dots \dots O_{k-1,j}O_{k,j}) \quad (1.2)$$

For every Particular Vector $I_V = O_V$

Circuits are considered to be reversible if they have an identical number of inputs and outputs, as well as a mapping that corresponds one-to-one between vectors of input and output. As shown in figure1. given below.

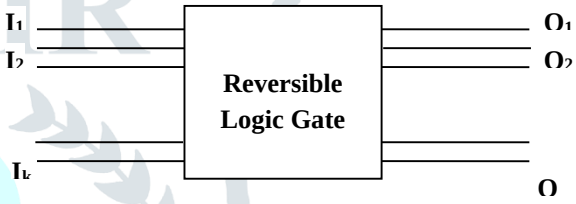

Fig. 1. A gate with K input and Output is called K*K gate

The reversible logic being as a more alternative and traditional approach for irreversible logic gate circuits. Since reversible logic computing does not erase or lose information or data in the logical operation.

The NOT gate, which is an 11 gate, is most basic reversible gate. 22 gates include a controlled NOT (CNOT) gate. 3x3 reversible gate choices include PG, TR, TG, and FG, gates. 1x1 reversible gates have no quantum cost, while 2x2 reversible gates have. The most effective method to create any reversible gate is to combine 1x1 NOT gates (an inverter) with 22 Feynman gates. Reversible gates include the FG gate, also known as CNOT gate, and V, V+ (V+ is its Hermitian, and V is square root of NOT gate). The following equation gives characteristics of V & V+ quantum gates.

$$V \times V = NOT \quad (1.3)$$

$$V \times V^{+} = V^{+} \times V = I \quad (1.4)$$

$$V^{+} \times V^{+} = NOT \quad (1.5)$$

Computing the aggregate of CNOT, V+ gates, and V gates is a method for determining the quantum cost of a reversible gate. Figure 1.2 illustrates the relationship between the NOT gate and the CNOT gate (Controlled NOT gate).

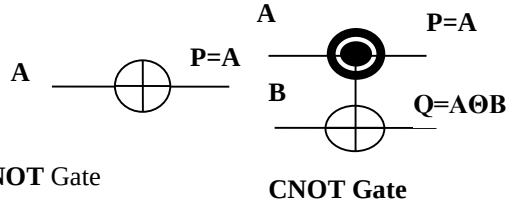

Fig. 2. 1x1 NOT Gate and CNOT Gate Logic Combination Diagram

(i) Garbage Input/output- The trash output of a reverse gate is a crucial characteristic since it refers to any input of a gate that is neither a principal output or an input to another gate. "Garbage" refers to gate's unneeded outputs. Every bit of trash produced comes with a hefty price tag. A reversible logic computing circuit of this kind might look like Figure 3 if its purpose were to calculate Ex-OR of two variables. To make the logic circuit reversible, this operation must create one more output, known as the trash or undesired output (P = A).

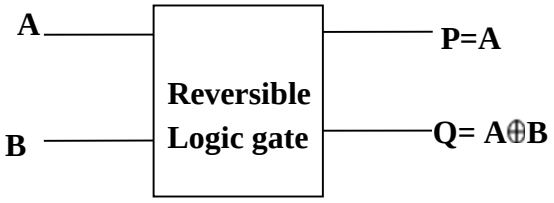

Fig. 3. Basic block of reversible logic gate with Garbage input/output

(ii) Quantum Cost- The input lines' constants may be either zero (0) or one (1), depending on circuit's needs. Gate Count represents function's number of reversible gates. The number of fundamental gates (EXOR, AND, and NOT gates) needed to easily synthesize given additional functions is referred to as hardware complexity.

(iii) Critical Path- Using the critical route, Delay may be computed in reversible logic. The optimal system output is obtained through the longest route.

(iv) Gate Count- Every reversible circuit only carries out reversible function.

(v) Transistor Count- the number of logical gates' transistors multiplied by number of transistors required to implement a reversible gate.

The literature has several examples of reversible gates. Peres Gate (PG), Fredkin Gate (FRG), Toffoli Gate (TG), Feynman Gate (FG), and Kinoshita Gate (KG) are most typical of these gates. There is no information in literature on quantum realizations of any of these gates. In terms of nanotechnology, only FG, PG, FRG, TG, and have been achieved.

IV. Proposed Reversible Multiplexer

The proposed design of reversible multiplexer design required the less number of transistors and the design implementation of the complex design of large logic gate circuitry. This is the most fundamental approach for every design of logic gate is the using pass transistor logic gate concept.

The proposed 2:1 Reversible MUX is realized using CMOS (i.e. PMOS and NMOS). 2:1 Reversible MUX producing two garbage bits i.e. G1 and G2. These are inputs: S, A, and B. Bits of message are sent to output Y based on selection input S. Suggested 2:1 Schematic Figures 4 and 5 depict transient response of a suggested 2:1 reversible MUX and the reversible MUX, respectively.

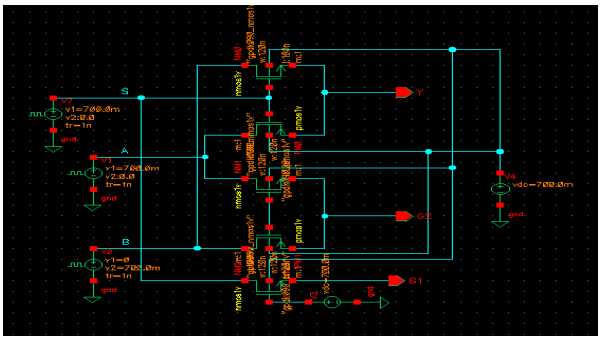

Fig. 4. Schematic of Proposed 2:1 Reversible MUX

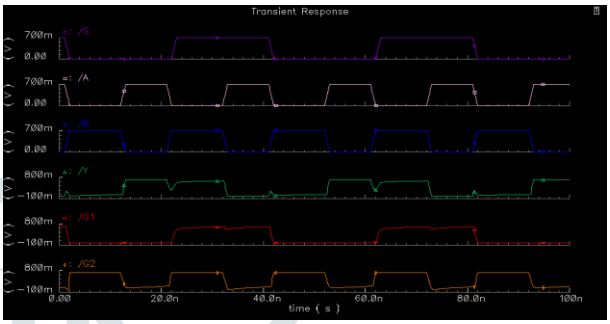

Fig. 5. Transient Response of proposed 2:1 Reversible MUX

The 2:1 Reversible MUX that is being suggested is implemented utilizing CMOS (i.e. NMOS & PMOS). The 2:1 Reversible MUX generates G1 and G2, 2 trash bits. S, A, and B are inputs. The bits of message that correspond to selection input S are sent to output Y. DC Response of 2:1 Figure 6 depicts reversible MUX, while Figure 7 displays waveform of leakage current.

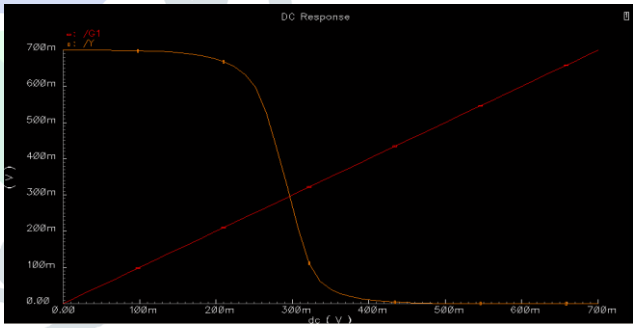

Fig. 6. DC Response of proposed 2:1 Reversible MUX

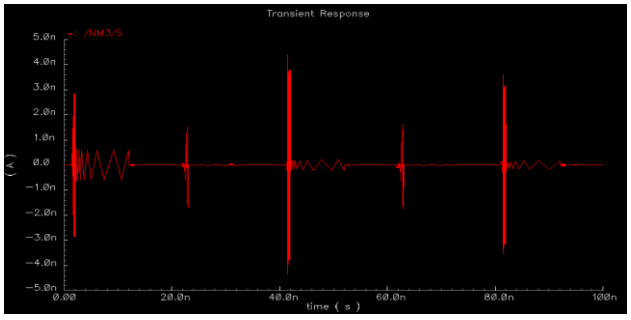

Fig. 7. LC Waveform of proposed 2:1 Reversible MUX

V. Reversible MUX Using DG FINFET Technique

COMS DG FINFET (CDF) system is connected to CMOS Reversible MUX (CRM). Here self-deciding control of back & front gate in CDF can be productively utilized to create execution and lessen control utilization. Self-determining gateway control may be used in non-obvious ways to join

parallel transistors. A parallel transistor pair consists of two transistors connected at their source and drain terminals. It is expected that the second gate, which is added backward to the standard CDF entrance, will largely regulate transient channel effects and leakage current. In short gate (SG) mode, the gates of transistors are connected; in IG mode, self-deciding digital signals drive gates of two devices; in LP (low power) and IP (ideal power) modes, back gate is connected to a turnaround inclination voltage for enhanced leakage control; and in crossover mode, LP and IG operations are combined. The constant downscaling of mass CMOS generates fundamental problems due to its base material. Scaling mass CMOS to 45nm gate lengths presents several issues, including gate dielectric leakage, ideal current, short channel effects, and device-to-device variances. However, CDF-based plans provide better control over short channel impacts, low spillage, and higher yield in 45nm aides that outperform scaling deterrents. Figure 8 depicts a schematic of a CDF coupled to a CRM. Figure 9 depicts CRM output waveform using CDF approach.

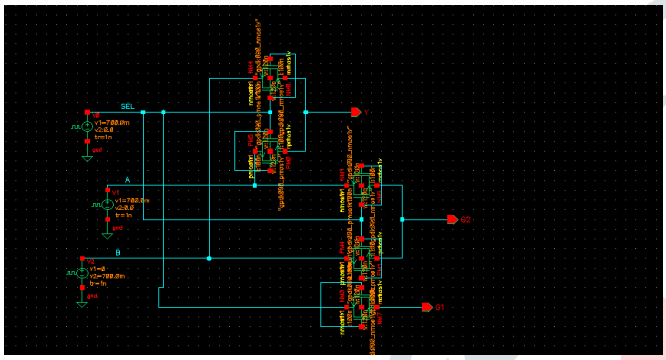

Fig. 8. Schematic of Proposed CRM using CDF

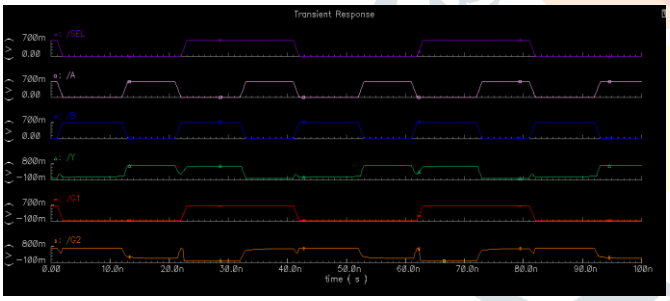

Fig. 9. Output waveform of Proposed CRM using CDF

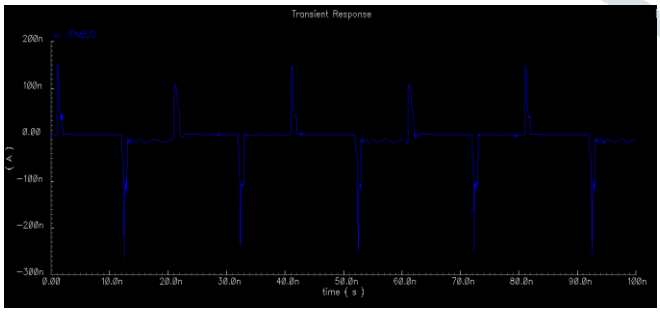

Fig. 10. LC waveform of Proposed CRM using CDF

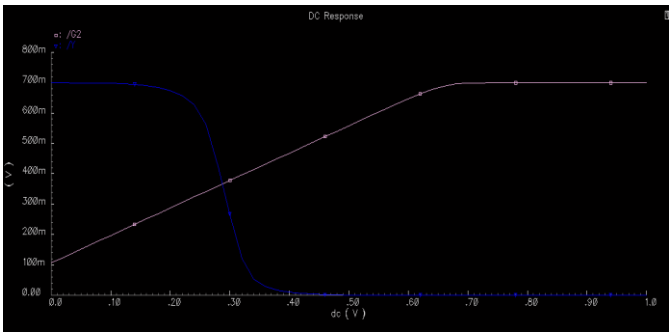

Fig. 11. DC Response of Proposed CRM using CDF

VI. Simulation Result

The cadence tool was used to simulate a CMOS reversible MUX (CRM) circuit, with a nominal supply voltage of 0.7 V and 90nm technology. Utilising 90 nm technology and a Vdd = 0.7 V nominal supply voltage, CRM simulations have been run utilizing cadence tool. At 27 degrees Celsius, when gate leakage is sole prominent mechanism, a CRM circuit's power consumption has been reduced in a number of ways without sacrificing performance. The parameters like leakage current & leakage power from a comparison of CRM Circuits utilizing CDF approach are shown in Table.1 below.

Comparison Result Summary for CRM Circuit utilizing CDF approach is shown below table

TABLE I. Simulated Result Summary

Performance Parameter	CMOS Reversible MUX (CRM)	CRM Circuit using CDF technique
Technology Used	90nm	90nm
Supply Voltage	0.7V	0.7V
Leakage Power	3.17nW	1.3nW
Leakage Current	4.53nA	1.1nA
Delay	2.11ns	1.2ns

TABLE II. Comparison shows with previous work

Performance Parameter	Previous work [26]	Proposed work
Supply Voltage	1.14 v	0.7v
Power	11.264 µW	3.17nW
Current	0.987mA	4.53nA
Delay	4.894ns	2.11ns

VII. Conclusion

Power dissipation may be minimized if the entire design is based only on reversible logic. The field of reversible logic has grown in popularity in recent years due to its advantageous characteristic of reduced power consumption. There are many forms of combinational circuits in this architecture, including RD (reversible decoder), RE (reversible encoder), RDM (reversible de-multiplexer), and RM (reversible multiplexer). When compared to older designs, the recommended CRM gate requires fewer constant inputs, garbage outputs, and reversible logic gates to perform its three distinct functions as a 4:2 encoder, 2:4 decoder & 1:2 de-multiplexer. This improves the proposed reversible MEDD gate's power consumption. At 90nm CMOS technology, power dissipation of a CRM gate is measured to be 3.17nW. Power is determined to be 1.3nW less when employing the CDF approach in comparison to CRM. This design serves as a starting point for creating more

complicated arithmetic systems employing these reversible logic gates, resulting in improved computing system performance.

REFERENCES

1) P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, A. Dandapat, Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit, 2014.
2) Z. Abid, H. El-Razouk, D. El-Dib, Low power multipliers based on new hybrid full adders, Microelectr. J. 39 (12) (2008) 1509–1515.
3) S. Goel, A. Kumar, M.A. Bayoumi, Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 14 (12) (2006) 1309–1321.
4) A. K. Bansala and A. Dixit. (2015). "Advances in logic device scaling," IETE Technical Rev. 32 (4), pp. 311–318.
5) I. Brzozowski, A. Kos, Designing of low-power data oriented adders, Microelectr. J. 45 (9) (2014) 1177–1186.
6) K. Navi, V. Foroutan, M. Rahimi Azghadi, M. Maeen, M. Ebrahimpour, M. Kaveh, et al., A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter, Microelectr. J. 40 (10) (2009) 1441–1448.
7) K. Navi, M. Maeen, V. Foroutan, S. Timarchi, O. Kavehei, A novel low-power full-adder cell for low voltage, Integration 42 (4) (2009) 457–467.
8) M. Vesterbacka, "A 14-transistor CMOS full adder with full voltageswing nodes," in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Oct. 1999, pp. 713–722.
9) R. Vaddi, et al. (2010). "Robustness comparison of DG-FinFETs with symmetric, asymmetric, tied and indepen-dent gate options with circuit co-design for ultra low power subthreshold logic," Elsevier Microelectron. J. 41(4), pp. 195–211.
10) N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley, 2010.
11) H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002
12) Samaali H, Perrin Y, Galisultanov A, Fanet H, Pillonnet G, Basset P (2019) MEMS four-terminal variable capacitor for low power capacitive adiabatic logic with high logic state differentiation. Nano Energy 55:277–287
13) Barla P, Shet D, Joshi VK, Bhat S (2020) Design and analysis of LIM hybrid MTJ/CMOS logic gates. 2020 5th International Conference on Devices, Circuits and Systems (ICDCS). IEEE, pp 41–45.
14) Gavaskar K, Malathi D, Dhivya R, Dimple Dayana R, Dharun I (2020) Low power design of 4-bit simultaneous counter using digital switching circuits for low range counting applications. 2020 5th International Conference on Devices, Circuits and Systems (ICDCS). IEEE, pp 316–320.
15) Swami N, Khatri B (2020) High performance CMOS circuit design. AIP Conference Proceedings 2220:020187. https://doi.org/10. 1063/5.0002200
16) Schmickl S, Faseth T, Pretl H (2020) An RF-energy harvester and IR-UWB transmitter for ultra-low-power battery-less biosensors. IEEE Trans Circuits Syst I: Regular Papers 67(5):1459–1468.
17) Himanshu Thapliyal and M.B Srinivas, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate", IEEE International Conference on Computer Systems and Applications, pp.100 - 103, 2006.
18) Nidhi Pokhriyal, Harsimranjit Kaur and Neelam Rup Prakash, "Compressor Based Area-Efficient Low-Power 8x8 Vedic Multiplier", International Journal of Engineering Research and Applications, Vol. 3, Issue 6, pp.1469-1472, 2013.
19) Maryam Ehsanpour, Payman Moallem and Abbas Vafaei, "Design of a Novel Reversible Multiplier Circuit using Modified Full Adder", IEEE International Conference on Computer Design and Applications, Vol. 3, pp. 230-234, 2010.
20) Madhusmita Mahapatro, Sisira Kanta Panda, Jagannath Satpathy, Meraj Saheel , M.Suresh, Ajit Kumar Panda and M K Sukla, "Design of Arithmetic Circuits Using Reversible Logic Gates and Power Dissipation Calculation" International Symposium on Electronic System Design, pp. 85 - 90, 2010.
21) Anindita Banerjee and Anirban Pathak, "Reversible Multiplier Circuit" Third International Conference on Emerging Trends in Engineering and Technology. pp.781-786, 2010.
22) M. Jenath and V. Nagarajan "FPGA Implementation on Reversible Floating Point Multiplier ", International Journal of Soft Computing and Engineering, Vol.2, Issue-1, pp. 438-443, 2012.
23) Kartikeya Bhardwaj and Bharat M. Deshpande, "K-Algorithm: An Improved Booth"s Recoding for Optimal Fault-Tolerant Reversible Multiplier", IEEE International Conference on VLSI Design, pp. 362-367, 2013.
24) Pradip Panchal, Palak Patel,Vandit Thakkar and Rachna Gupta, "Pose, illumination and expression invariant face recognition using Laplacian of Gaussian and Local Binary Pattern", 5th Nirma University, IEEE International Conference on Engineering (NUiCONE), pp. 1-6, 2015.
25) Bilel Ameur, Sabeur Masmoudi, Amira Guidara Derbel,and Ahmed Ben Hamida "Fusing Gabor and LBP feature sets for KNN and SRC-based face recognition", 2nd IEEE International Conference on Advanced Technologies for Signal and Image Processing (ATSIP), pp 453 - 458, 2016.
26) Shayida Syed, Md.Mohasinul Huq and Mohan Das, "Implementation Of Reversible Combinational Multiplxers Using Reversable Gates", JES (Jounral of Engineering Science) Vol 10, Issue 12, Dec/2019.