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DEVELOPMENT OF AN ENERGY EFFICIENT TIQ FLASH ADC USING TANNER EDA TOOL

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Abstract: A new method for increasing the effectiveness of flash ADC devices is the Threshold Inverter Quantizer (TIQ). This is accomplished by doing away with the need for a resistive or capacitive voltage divider circuit, a set of differential comparators, and reference voltage generator. Instead, it uses a Complementary Metal Oxide Semiconductor (CMOS) inverters are used to produce the internal reference comparator array. Significant enhancements in power consumption, silicon area, and operating speed are achieved by using the inverters threshold voltage referred as the reference voltage. However, the inverter threshold voltages sensitivity for changes in operating temperature and process conditions calls for a compensation strategy. This study introduces a TIQ-based flash ADC that incorporates voltage adjustment for the inverter threshold. The project's aim is to create adding a mux-based encoder that uses transmission gate logic and modifying the TIQ comparator using power gating, a 5-bit flash ADC is achieved. The design and simulation of this system are performed using TANNER EDA in a 180nm technology process.

Keywords:

Mux based encoder, TIQ comparator, Power gating

I. INTRODUCTION

Digital Signal processing offers multitude of results across various digital platform, such as increased design flexibility, programmability, reduced silicon area, enhanced accuracy, and decreased power consumption. These advantages contribute to more cost-effective and expedited design processes, facilitating the development of systems with diminished size and increased speed. High-speed converters from analog to digital (ADCs) are particularly essential in applications like wireless both picture processing and communication.

In recent years, industry has been heavily influenced by the metal oxide semiconductor, making it challenging to design analog circuits that are compact, operate at lower supply voltages, and have shorter transistor channel lengths. Operational amplifiers (op-amps) play a crucial role in balancing performance parameters enabling handling various aspect ratios by adjusting transistor widths and lengths for optimal performance.

Designing digital systems with portable and long-lasting battery life is a desirable feature. Making programs that use less electricity will help achieve this. Given that ADCs are often integral components in mixed-signal systems, there is a focus on designing ADCs that are energy-efficient, thereby enabling higher speed. Various ADC architectures are available, including successive approximation (SAR), Flash, sigma-delta, and others. Among these, Flash ADCs are favored for their high speed due to their parallel

architecture, which is not constrained by resolution, making them ideal for systems requiring elevate bandwidth.

The conversion of Analog signals into digital signals and digital signal processing and computing is facilitated by Analog-to-digital converters, or ADCs. ADCs are characterized by three fundamental attributes that are established at the design phase: resolution, speed, and power consumption. The performance metrics of an ADC, encompassing its sampling rate, power consumption, and resolution, are intrinsically tied to its architectural design. Therefore, selecting the appropriate ADC for each specific application is crucial. Different types of ADCs are available, such as SAR, Dual Slope, Sigma Delta, and Flash ADCs. Among these, Flash ADCs are most commonly used due to their optimal balance between performance metrics. They are known for their fast performance, primarily because of their parallel architecture.

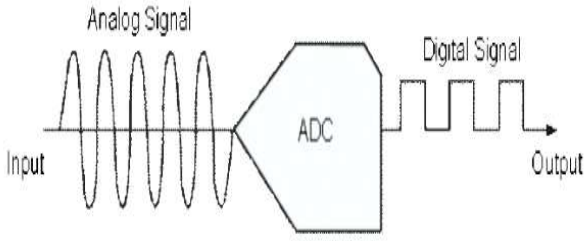

Fig1: Analog to digital conversion

A Transformation from Analog to Digital (ADC) serves as a crucial component that converts analog signals, such as voltage, into a digital format that can be processed by a microcontroller. While some microcontrollers incorporate built-in ADCs, others may require external ADCs. These external ADCs typically operate with a resolution of 8–10 bits, providing 256–1024 quantization levels. Microcontrollers with ADC capabilities often include multiplexed ADCs, allowing for the connection of more than one analog input channel. For instance, the PIC18F452 microcontroller includes 10-bit, 8-channel ADCs.

The ADC is an important tool with extensive applications in today's digitized world. Among various ADC types, the Flash ADC stands out for its high speed. It comprises 2N comparators that generate thermometer-coded outputs, which are then encoded into digital outputs by an encoder. In elevate-tempo applications, the comparator's role is crucial, and minimization techniques are employed to enhance its performance. Flash ADCs face a notable challenge due to their high power consumption, prompting the development of low-power Flash ADCs equipped with low-power comparators. The design aspects that need to be considered include gain, phase & power dissipation. A simple two-stage comparator with high gain can be made using an op-amp with a Miller capacitance, providing the benefit of low power operation.

To address the issue of low power consumption, methods like clock and power gating, transistor stacking are used. Static power consumption primarily results from leakage currents in MOSFET devices, which flow even when the transistor is off. This significantly affects the threshold voltage of transistors in the circuit. To mitigate this, scholars have proposed power gating techniques, including the use of a Mux-based encoder in transmission gate logic using the lector approach. This method involves stacking MOS two LCTs, one is close to CMOS gate's cutoff region of operation, are introduced into the path from Vdd to Gnd. This approach significantly reduces leakage power by effectively shutting off power to the circuit.

II. LITERATURE REVIEW

ADCs play an important part in the digital era, catering to a wide array of applications. Among the fastest ADCs, Flash ADCs stand out, yet they consume a significant amount of power. This study focuses on creating high-speed, medium-resolution Flash ADCs using an ultralow-voltage design approach to improve energy efficiency. By lowering the voltage supply, the power consumption of a digital system can be decreased, albeit at the cost of increased delay time. To address this, a voltage boosting comparator with forward body biasing is employed, utilizing 45nm CMOS technology to design a Flash ADC operating in the ultra-low-voltage (ULV) domain. This approach minimizes power consumption by maintaining the delay time relatively stable as the supply voltage is reduced. Offset compensation is achieved through the body-bias calibration technique [1].

S.Veeramachanen, A.M. Kumar, V. Tummala and M.B. Srinivas:

This study introduces a low-power, adaptive flash ADC that offers exponential power reduction alongside a linear reduction in resolution. The design includes a feature where Inactive voltage comparators which are in parallel are set to sleep mode to minimize power usage, mainly drawing leakage power. [2].

Sarojini Mandal, Dr. J.K .Das:

The Flash architecture is renowned for its rapid Analog to Digital conversion speed. This paper introduces a Flash type ADC. Various types of thermometer to binary encoders are employed and evaluated in terms of delay and power consumption. Flash type ADCs typically consume considerable power, thus utilizing comparator with low power aims reducing device consuming power, especially since it employs maximum comparators. [6].

Pradeep Kumar, Amisha, P. Naik:

The 3-bit flash ADC exhibits certain limitations, such as its accuracy in converting analog voltage to digital form, which is confined to an amplitude range of 0 to 3 volts. Despite these limitations, the simplicity of this architecture allows for potential expansion to medium-to-high resolution applications [9].

Ashima Gupta, Anil Singh:

Parallel ADCs are fastest type due to their ability of carrying out the conversion in a single step. Particularly suited for applications that demand high bandwidth. The comparators output, in the form of thermometer code, must be translated into binary code using an appropriate encoder. A significant design challenge in low-power Flash ADCs is minimizing the power dissipation of the encoder. Multiplexer-based encoder stands out for its power efficiency and simplicity, making it the most appropriate choice for low-power Flash ADC design [10].

III. EXISTING METHOD

Analog to digital converter is a crucial requirement for microprocessors, microcontrollers, DSP architectures, communication devices, and consumer electronics, serving as a bridge between analog and digital signal processing. It enables the conversion of real-world analog signals into digital data, facilitating rapid and precise processing in high-performance digital devices. Among various ADC types, Flash ADCs are distinguished for their speed and simultaneously compare the analog input voltage against reference voltages.

The type of ADC is crafted using TIQ (Three-Input Quadrature) comparator. This design includes a threshold-adjusted TIQ module with three CMOS inverter circuits. The system utilizes a DC feedback path to automatically adjust the inverter's threshold voltage. The self-tuning threshold mechanism uses resistances(R0 and R1) for establish the threshold voltage for both primary, secondary inverters. TIQ comparator's central component is the primary inverter, which are designed using NM3 and PM3 connected to the power rails. NMOS and PMOS works in linear mode, forming a feedback system. Their gate terminals are managed by the primary inverter's output, effectively functioning as voltage-controlled resistors. Transistors resistances are regulated by primary inverters output voltage.

The secondary inverter replicates the design of the primary inverter, preserving identical proportions. By setting its input to match the desired threshold voltage, primary inverter produces required controlled voltage to control MOSFETs two resistances which is connected to power rails. This feedback path acts as self-regulating system, ensuring that the switching thresholds of both the primary and secondary inverters remain consistent, regardless of fluctuations in process or temperature.

If master inverter output voltage falls below the specified level, it might be attributed to process or temperature fluctuations. This causes the NMOS resistance (NM3) to increase and that of PMOS (PM3) to decrease. As a result, the inverter's switching threshold gradually increases towards the desired value due to resistance changes towards its power rails. Until the threshold equals the intended value, this negative feedback loop keeps going. On the other hand, the circuit uses the same negative feedback process to modify its threshold to match if the switching

threshold exceeds the intended value. PM4 and NM4 are impacted by changes in resistance, which the slave inverter replicates from the master inverter.

The circuit's capacity to self-correct the threshold voltage of inverter stabilizes the comparators reference voltage, which is a significant benefit. This removes the requirement for the ADC to be calibrated at startup or during operation. The TIQ Comparator converts the analog input signal into a Unary coding, which then converted into binary code. Since this is a 5-bit flash ADC, it requires a 32-bit TIQ Comparator array and a 32-bit mux-based encoder circuit.

The overall adc architecture is shown below.

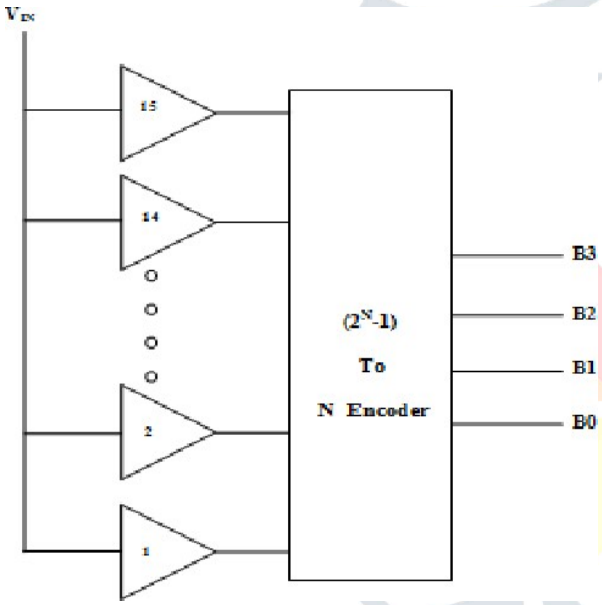

Fig2: Flash ADC

IV. PROPOSED METHOD

This section looks at using a Mux-based encoder with transmission gates and the TIQ comparator in conjunction with the Power Gating Technique. The performance of the ADC is intended to be enhanced by these changes, particularly with regard to power efficiency.

Introduction to Power Gating Technique:

By turning off the power supply to particular circuit blocks while they are not in use, a technique known as "power gating" is used in integrated circuits to lower power usage. These days' chips, which frequently have a large number of functional blocks that might not be constantly active, benefit greatly from this strategy.

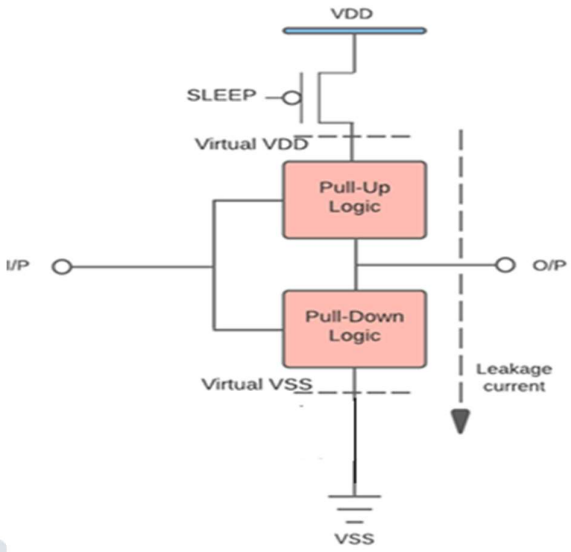

Fig3: Schematic representation of the Power Gating Method

The approach known as "power gating" involves adding switches, which a power management unit may toggle, to the power supply lines of particular circuit portions. By turning off the switches, the power supply is shut off and the circuit's power consumption is decreased while certain circuit portions are not in use. To further reduce power consumption in integrated circuits, this technique is frequently used in conjunction with other techniques for power management, like dynamic frequency and voltage scaling (DVFS). Power gating implementation, however, can provide difficulties, such as heightened complexity and potential timing problems during power state transitions. Power gating is commonly employed in contemporary electronic devices such as laptops, cellphones, and other portable electronics and is a very effective method of managing power consumption in integrated circuits, despite these difficulties.

TIQ comparator:

In this project, a Flash ADC is created using a TIQ (Three-Input Quadrature) comparator. The schematic shows a threshold-adjusted TIQ module that includes three CMOS (Complementary Metal-Oxide-Semiconductor) inverter circuits. This setup uses a DC feedback path to automatically adjust the inverter Vth, ensuring precision and dependability.

The self-tuning threshold mechanism is shown below. It uses a resistive divider, made up of for the primary and secondary inverters, use R0 and R1 to set the Vth. A transistor NM3 & a transistor PM3 connect the primary inverter, which is the central component of the threshold-adjusted TIQ comparator, to the power rails. In their linear (triode) state, these feedback mechanism is facilitated by transistors. They are essentially voltage-controlled resistors, with their gate terminals under the primary inverter's output control. The Vout of primary inverter regulates these transistors' resistances.

The secondary inverter mirrors the design of the primary inverter, maintaining identical proportions. By setting its input to match the desired threshold voltage, The power rails are connected to two MOSFETs, and the primary inverter produces the control voltage required to regulate their resistance. This feedback loop acts as a self-regulating system, ensuring that the switching thresholds of both the primary and secondary inverters stay consistent, regardless of variations in process or temperature.

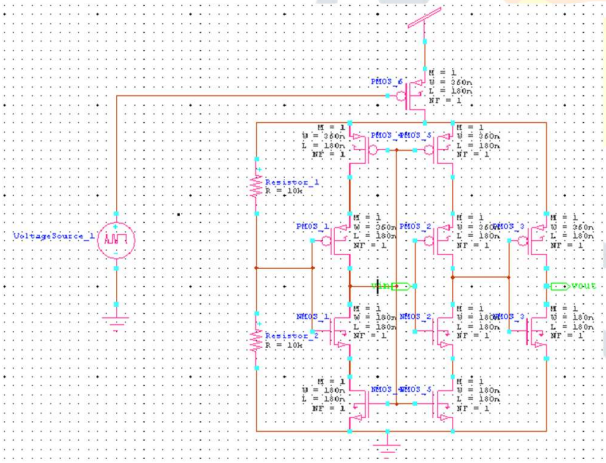

Fig4: Schematic of proposed TIQ comparator using power gating

In this design, an extra PMOS transistor is introduced to disrupt the power source for the circuit path from VDD to GND. This action is intended to decrease power consumption. The operation of this additional transistor is governed by a pulse voltage source input signal.

Mux based encoder:

The diagram below illustrates the structure of a Mux-based encoder. In this scenario, we're developing a 2x1 Mux utilizing transmission gate logic. Suppose you aim to construct a 2-to-1 mux with the select line S, the in A &B, and the out Y. The behavior of the mux is as follows: when S is at low state (0), Y output mirrors input A. Conversely, S is at a high state (1), the Y output tracks input B. Transmission gate situated between A and Y is manipulated by the signal S. When S is high (1), the gate permits the signal from B to pass through, resulting in Y outputting B. In the case of S being low (0), the gate obstructs the signal from B, causing Y to follow A. Transmission gate logic is frequently employed in the design of integrated circuits to achieve efficient and compact designs. It's important to acknowledge that while transmission gates provide benefits such as minimal voltage drop and bidirectional signal transmission, they also present challenges, including leakage current and potential signal distortion.

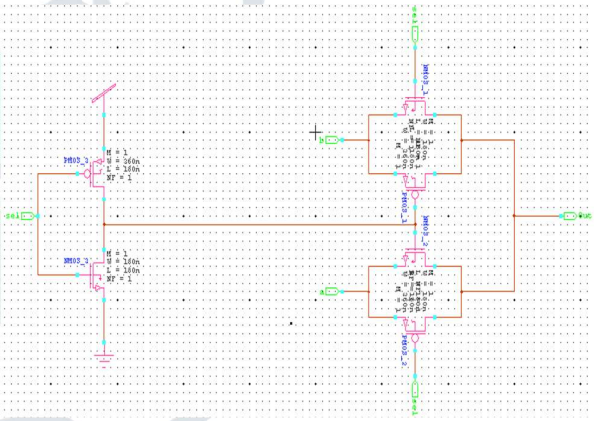

Fig5: Mux using Transmission gate

A mux-based encoder basically digital circuitry which transforms multiple signals of input into reduced number of output signals, utilizing multiplexers (muxes) for this encoding process. Based on a series of control or select lines, a multiplexer basically data selector device which selects between several input signals chooses one and routes it to a single output line.

INTRODUCTION TO LECTOR APPROACH:

In CMOS technology, the process of voltage scaling, which involves reducing the threshold voltage, inadvertently increases subthreshold leakage current, leading to higher static power dissipation. To address this issue, we introduce a novel approach named LECTOR, designed for the

creation of CMOS gates. This method significantly reduces absence of leakage current elevating dissipation of dynamic power. The LECTOR technique incorporates two LCTs within the logic gate, one p-type and one n-type. It is the source of each LCT that controls its gate terminal, providing a unique mechanism to control and minimize leakage current.

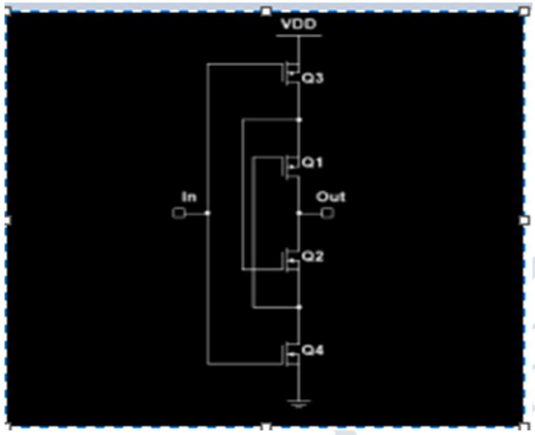

Fig6: INVERTER USING LECTOR

For every possible combination of inputs, A LCTs in this configuration "Near its Cutoff Voltage" at all times. This results in a considerable reduction in leakage currents by raising the path's resistance from VDD to GND. To create a leakage-controlled circuit, LCTs are added after the gate-level netlist of the provided circuit is transformed into the implementation of a static CMOS complex gate. Among other techniques, LECTOR's superior leakage reduction comes from its ability to function well throughout the circuit's active and idle phases.

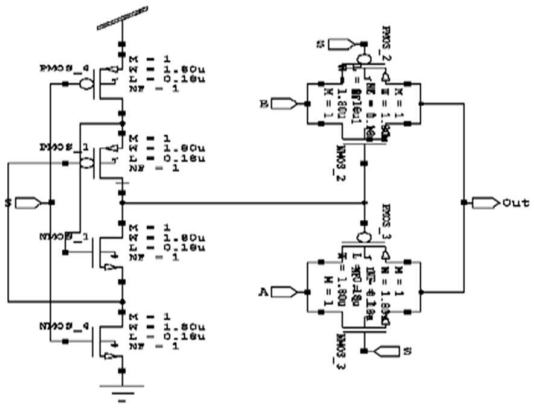

Fig7: schematic of a 2:1 Mux with a lector approach that uses transmission gate logic.

In this schematic, lector approach used in CMOS employed in the circuit. Basically, Method that uses little power is the lector approach. Effective transistor stacking in the VDD to GND path is the fundamental concept underlying our leakage power reduction strategy. "Compared When several transistors are off in a path from VDD to GND, it is far less leaky than a state." By introducing within every CMOS gate, there are two leakage control transistors (LCTs). we can achieve our desired effect by placing one LCT close to its cutoff region of operation.

Here is a simplified explanation of how a mux-based encoder operates:

1. Inputs: The encoder accepts multiple input lines, each representing a unique input combination.

2. Selection Lines: The select lines by the mux is determined by the number of input lines. For n input lines, log2(n) select lines are needed.

3. Encoding Logic: The select lines are activated by the input lines. The specific combination of select lines determines which input is active.

4. Output: Mux output corresponds to the selected input line, representing the encoded value for that specific input combination.

Multiplexers are versatile devices that can be used in both digital and analog applications, serving as fast-acting switches that connect multiple input lines to a single output line based on control signals. They are fundamental components in digital logic design, enabling the efficient routing of data and the creation of complex logic functions.

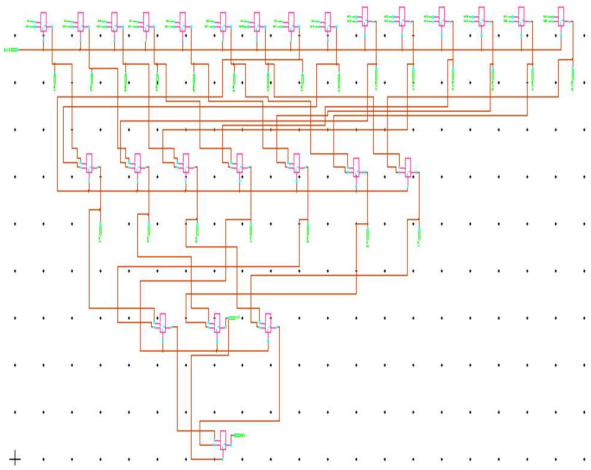

Fig8: Schematic of Mux based encoder

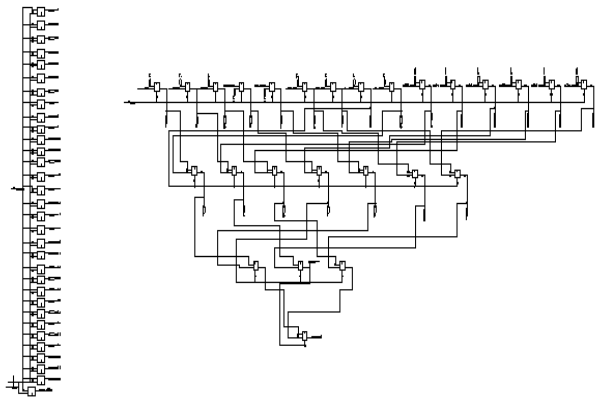

Fig9: Utilised are a Mux-based encoder and a modified TIQ comparator in the structure of the suggested flash ADC.

V. RESULT AND ANALYSIS

A thorough assessment of the suggested TIQ structure using S-edit in Tanner EDA is provided in the Results and Discussion section. Prior to beginning the T-Spice simulation phase, a meticulous design process was implemented to guarantee that no schematic errors or connections were made. This simulation included crucial steps like incorporating a technology file, determining the simulation duration, defining input sources, and adding instructions for calculation of power and delay. Selecting "run simulation" began the simulation.

After it was finished, the suggested Full adder structure's performance was assessed in a variety of circumstances by carefully analyzing the waveforms. MOSFET use, power metrics, and delay metrics were all carefully examined in this process. Waveform analysis provided a thorough examination of the functionality and performance characteristics of the suggested structure by shedding light on its dynamic behaviour.

The efficiency and resource allocation of the

suggested FF structure were revealed by the examination of MOSFET consumption. Examining power levels made it easier to evaluate the characteristics of power consumption, which is important for determining how energy-efficient the suggested design is. Delay values were also examined in order to gain insight into the operating speed and responsiveness of the transmission gates-based Mux-based encoder and the suggested proposed method that uses the Power Gating Technique.

The Result & Discussion section serves as a comprehensive analysis of the Proposed TIQ comparator structure, integrating simulation outcomes with insightful discussions to describe the design's overall performance as well as any possible areas for development.

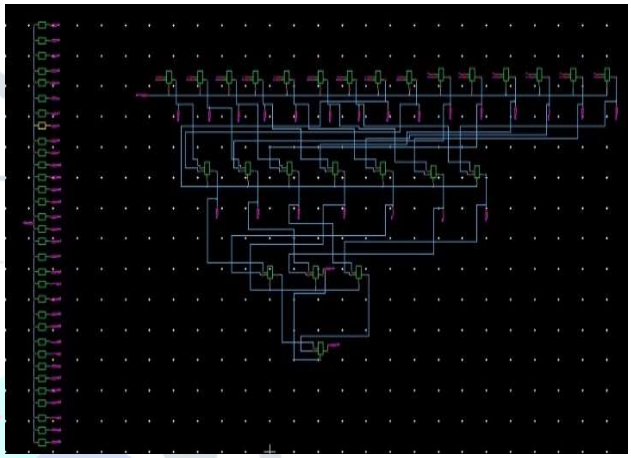

Figure10 : Schematic of proposed full adder

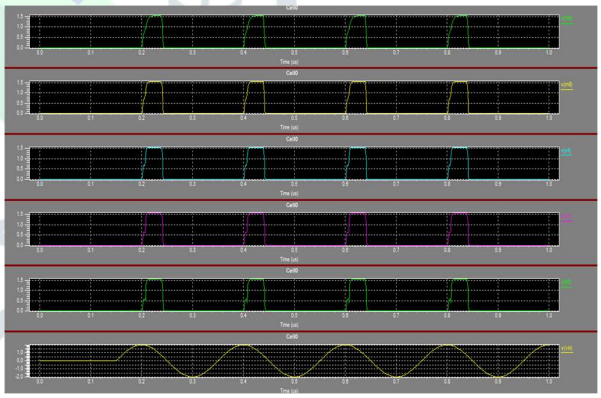

Figure11 : SIMULATION WAVEFORM

COMPARISION TABLE:

	Area	Power	Delay
Existing	632	7.1327mw	2.0062ns
Proposed	508	2.0808mw	1.2818ns

In existing method the output values of the delay and power value is 2.0×10^{-9} & 7.13×10^{-6} while we try to reduce the delay & power we use technique as "Power Gating technique and Lector approach". Using Power Gating technique and Lector approach we have observed that area (transistors count) and power got decreased.

CONCLUSION

ADCs are essential components in a wide range of applications that bridge the gap between analog and digital domains, leveraging the computational advantages of digital processing. As the digital processing paradigm continues to outpace traditional analog signal processing, the significance of ADCs in facilitating this transition becomes increasingly crucial. A specific type of ADC, known as the Flash ADC or Direct Conversion ADC, employs a set of comparators operating in parallel to achieve rapid data conversion rates. The paper explains the circuit of Flash ADC, utilizing a Transmission Gate configuration encoder using mux, comparator circuit with TIQ modifications &lector approach. The designs were executed using 180 nm technology within the Tanner EDA environment.

Future Work

The proposed approaches can be combined or used individually to achieve the desired performance objectives. Future research can explore the application of proposed model and used in several techniques.

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