Design of high speed 4x4 VedicMultiplier

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***ABSTRACT* - The escalating demand for high-speed processors underscores the critical need for efficient multipliers within fast processing systems. While addition and subtraction operations may be relatively straightforward, multiplication poses significant challenges due to its requirement for substantial hardware resources and processing time. Conventional multipliers often suffer from high latency and considerable power consumption, highlighting the urgency for innovative solutions.**

The development of a high-speed multiplier-and-accumulator (MAC) based on the Vertically & Crosswise method of Vedic mathematics. This method, renowned for its versatility across diverse multiplication scenarios, streamlines the generation of partial products and their summation in a single step. By leveraging VHDL for coding and the Xilinx ISE12.1i tool for synthesis and simulation, the proposed high-speed multiplier-and-accumulator (MAC) design with outperforms conventional multipliers in terms of speed.

Keywords- *Multiplier-and-Accumulator (MAC), Vedic Multiplication, Urdhva Tiryakbhyam Sutra.*

I. INTRODUCTION

Multipliers play a crucial role in a variety of computing applications, including microprocessors, digital signal processors (DSPs), and communication systems. However, as the need for higher processing speeds grows, the traditional approach of using a multitude of adders for partial product addition becomes inefficient, resulting in increased power consumption and slower performance.

To meet the demand for faster and more power-efficient multipliers, the Vedic multiplication technique presents an innovative solution. This technique draws from 16 Vedic sutras or aphorisms, offering concise formulas for solving mathematical problems with remarkable speed and efficiency. By leveraging the Vedic Method, computational speed in processors can be significantly improved while requiring fewer hardware resources.

This paper focuses on the design and implementation of a 4x4 bit Vedic multiplier, employing the Urdhva-Tiryakbhyam sutra, commonly known as the Vertically and Crosswise technique, from Vedic Mathematics. Utilizing Electronic Design Automation (EDA) tools, the hardware architecture of both 2x2 and 4x4 bit Vedic multipliers is explored, showcasing their effectiveness in practical applications.

The paper unfolds in a structured manner: Section I provides an in-depth explanation of the Vedic multiplication technique, outlining its fundamental principles. Following this, Section III delves into the hardware architecture of the 2x2 and 4x4 bit Vedic multipliers, demonstrating their implementation based on the principles of Vedic multiplication. Section IV illustrates the implementation and result of Vedic multiplier module used in High-Speed Multiplier-And-Accumulator (MAC) so obtained while Section V comprises of Conclusion followed by Acknowledgment and References.

II. ANCIENT VEDIC METHODS

The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

A. Vertically & Crosswise Technique

The proposed High-Speed Multiplier-And-Accumulator (MAC) draws its foundation from the "Urdhva Tiryakbhyam" sutra, an ancient algorithm traditionally utilized for decimal number multiplication. In this study, we adapt these principles to the binary number system, ensuring compatibility with digital hardware. This algorithm, known for its versatility, serves as a universal multiplication formula suitable for all scenarios, aptly named "Vertically and Crosswise."

The innovative concept underlying this algorithm enables the concurrent generation and addition of partial products, facilitating efficient multiplication operations. Moreover, its scalability allows for the extension to an n x n bit number format. Importantly, due to the parallel computation of partial products and their sums, the multiplier operates independently of the processor's clock frequency. A distinct advantage of this sutra-based multiplier lies in its efficient scalability. As the number of bits increases, the gate delay and area requirements exhibit gradual growth compared to conventional multipliers. These characteristic positions the proposed MAC as a compelling choice for high-speed computing applications, offering enhanced performance while minimizing resource utilization.

To illustrate this scheme, let us consider the multiplication of two decimal numbers 252 * 846 by Urdhva Tiryakbhyam method as shown in Figure 1. The digits on the both sides of the line (say, 2 and 6) are multiplied (6 x 2 = 12) and added with the carry from the previous step (initially, carry=0). This generates one of the bits of the result (i.e. 2) and a carry (i.e. 1). This carry (1) is added in the next step and hence the process goes on. If more than one line is there in one step, all the results are added to the previous carry. In each step, Least Significant Bit (LSB) acts as the result bit and all other bits act as carry for the next step. Initially the carry is taken to be zero.

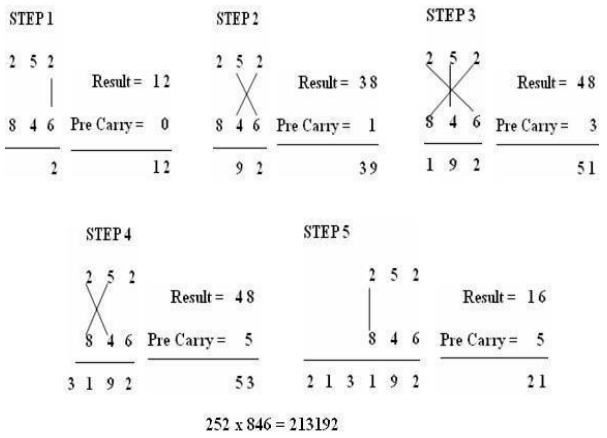


Figure 1: Multiplication of two decimal numbers 252 * 846

III. PROPOSED VEDIC ARCHITECTURE

The hardware architecture of 2x2 and 4x4 bit Vedic multiplier(VM) modules are displayed in the below sections. Here, "Urdhva-Tiryakbhyam" (Vertically and Crosswise) sutra isused to propose such an architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are doneconcurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay.

A. Vedic Multiplier for 2x2 bit

The method is explained below for two, 2-bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0 as shown in Figure 2. Firstly, the Least Significant Bits are multiplied which gives the LeastSignificant Bit (LSB) of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is thethird corresponding bit and carry becomes the fourth bit of thefinal product.

$$s0 = a0b0; \quad (1)$$

$$c1s1 = a1b0 + a0b1; \quad (2)$$

$$c2s2 = c1 + a1b1; \quad (3)$$

The final result will be *c*2*s*2*s*1*s*0. This multiplicationmethod is applicable for all the cases. The 2x2 bit Vedicmultiplier (VM) module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Figure 3.

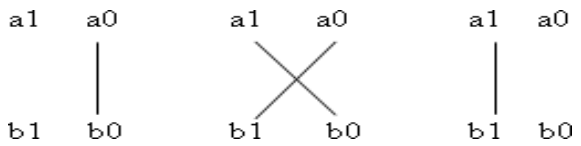
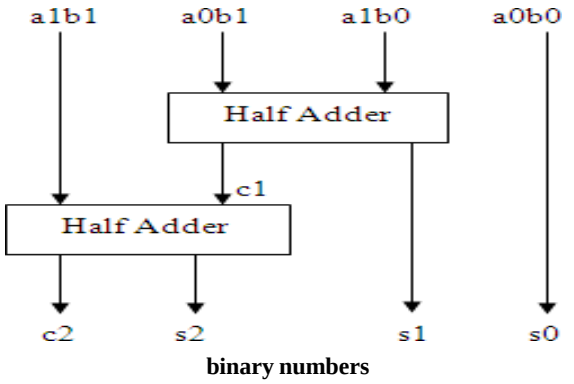


Figure 2: The Vedic Multiplication Method for two 2-bit



binary numbers

Figure 3: Block Diagram of 2x2 bit Vedic Multiplier (VM)

The same method can be extended for higher no. of input bits (say 4). But a little modification is required as discussed in section 3.2. This section illustrates the implementation of 4x4 bit VM which uses 2x2 bit VM as a basic module.

B. High-Speed Multiplier-And-Accumulator (MAC) using Vedic Multiplier

Divide the no. of bits in the inputs equally in two parts. Let's analyze 4x4 bit multiplication, say multiplicand A=A3A2A1A0 and multiplier B= B3B2B1B0. Following are the output line for the multiplication result, S7S6S5S4S3S2S1S0. Let's divide A and B into two parts, say "A3 A2" & "A1 A0" for A and "B3 B2" & "B1B0" for B.
Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for 4x4 bit multiplication as shown in Figure 4.

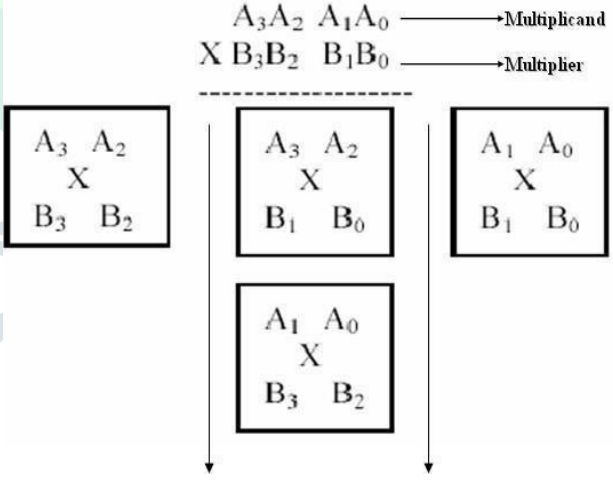


Figure 4: Structure for 4x4 bit Multiplication

Each block as shown above is 2x2 bit multiplier. First 2x2 multiplier inputs are "A1 A0" and "B1 B0". The last block is 2x2 bit multiplier with inputs "A3 A2" and "B3 B2". The middle one shows two, 2x2 bit multiplier with inputs "A3A2" & "B1B0" and "A1A0" & "B3B2". So the final result of multiplication, which is of 8 bit, "S7S6S5S4S3S2 S1S0".

To understand the concept, the block diagram of 4x4 bit Vedic multiplier is shown in Figure 5. To get final product S7S6S5S4S3S2S1S0 four, 2-bit Vedic multiplier (Figure 3)

and three 4-bit Carry Lookahead (CLA) Adders are required. In this proposal, the first 4-bit CLA Adder is used to add two 4-bit operands obtained from cross multiplication of the two middle 2x2 bit multiplier modules. The second 4-bit CLA Adder is usedto add two 4-bit operands, i.e. concatenated 4-bit ("00"& mostsignificant two output bits of right hand most of 2x2 multiplier module as shown in Figure 5) and one 4-bit operand we get as the output sum of first RC Adder. Its carry "ca1" is forwarded to third CLA Adder. Now the third 4-bit CLA Adder is used to addtwo 4-bit operands, i.e. concatenated 4 - bit (carry ca1, "0" & most significant two output sum bits of 2nd CLA Adder as shownin Figure 5) and one 4-bit operand we get as the output sum of left hand most of 2x2 multiplier module. Early literature speaks about Vedic multipliers based on array multiplier structures. The arrangement of Ripple Carry Adder as shown in Figure 6 helps us to reduce delay.

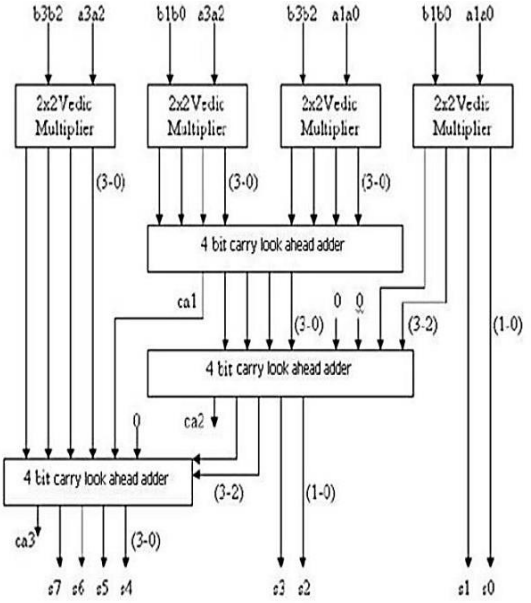


Figure 5: Block Diagram of High-Speed Multiplier-And-Accumulator (MAC) using 4x4 bit Vedic Multiplier (VM)

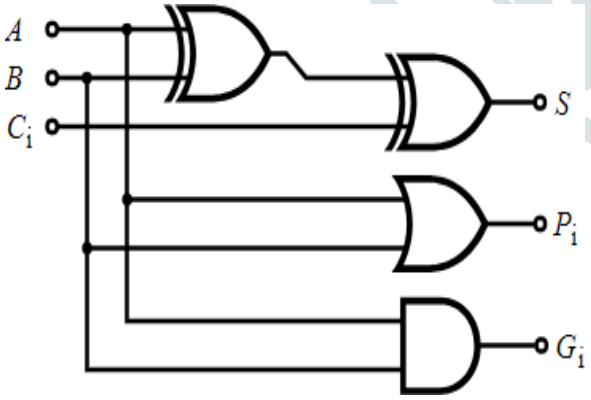


Figure 6: Circuit Diagram of Partial Full Adder

IV. IMPLEMENTATION & RESULTS

In this study, we implemented a High-Speed Multiplier-And-Accumulator (MAC) utilizing a 4x4 bit Vedic multiplier (VM) based on the "Urdhva Tiryakbhyam" Sutra. The design was realized in VHDL (Very High-Speed Integrated Circuit Hardware Descriptive Language), and logic synthesis and simulation were conducted using the XilinxISE12.1i EDA (Electronic Design Automation) tool suite, specifically employing the Project Navigator for synthesis and the ISim simulator for simulation.

Table 1 presents a comparison of synthesis results between the proposed Vedic multiplier and conventional multipliers in terms of time delay measured in nanoseconds. The combinational path delay achieved for the 4x4 bit Vedic multiplier is recorded at 6 ns. For reference, synthesis results for 4x4 bit Array and Booth multipliers, as reported by Umesh Akare et al [16], are included. The performance assessment is conducted on the Xilinx XC7A350T/FFG1156 device family, utilizing package tq144 and speed grade -5

Table 1 Comparison of Multipliers (in nanosecond)

Device: XC7A350T/FFG1156	Array Multiplier	Booth Multiplier	Vedic Multiplier
4x4 bit VM	32.001 ns	16.276 ns	**6.695ns**

The RTL (Register Transfer Level) schematic of the 4x4 bit Vedic multiplier comprises of four 2x2 bit Vedic multiplier (vedic2by2) v1, v2, v3, v4 and three 4-bit CLA Adder(cla_adder) c1, c2, c3 as shown in Figure 7 while the simulation resultsobtained are shown in Figure 8 for verification. In behavioral simulation we have tested for input bits: - "0100" (in decimal number system 4) and "0100" (decimal number system 4) as inputs and the output=00010000, indicates the final 8-bit result.

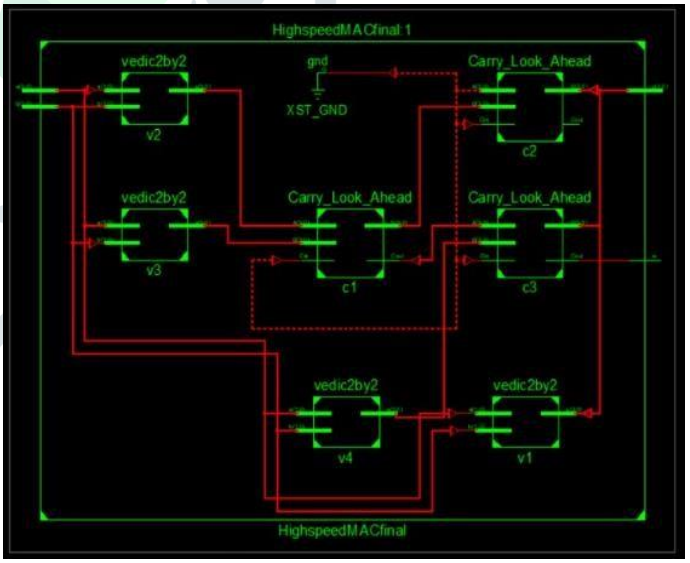


Figure 7: RTL schematic of High-Speed Multiplier-And-Accumulator (MAC) using 4x4 bit Vedic Multiplier

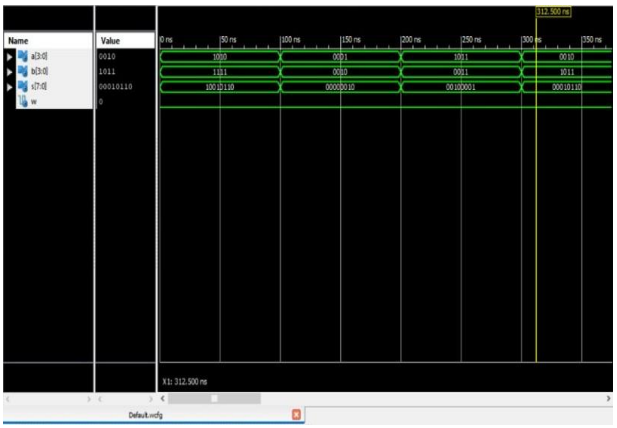


Figure 8 Simulation result of binary 4x4 bit Vedic Multiplier

Table 2: Area utilization summary report

Area utilization	Nos.
EXors	32
1-bit xor2	32
BELS	24
LUT2	2
LUT4	8
LUT5	1
LUT6	13
IO Buffers	17
IBUF	8
OBUF	9
Number of LUT Flip Flop pairs used	24
Number with an unused Flip Flop	24 out of 24 100%
Number with an unused LUT	0 out of 24 0%
Number of fully used LUT-FF pairs	0 out of 24 0%
Number of unique control sets	0
Number of IOs	17
Number of bonded IOBs	17 out of 600 2%

V. CONCLUSION

This paper introduces a novel High-Speed Multiplier-And-Accumulator (MAC) design, leveraging the "Urdhva Tiryakbhyam" Sutra from Vedic Mathematics. The proposed MAC architecture employs a 4x4 bit Vedic multiplier and notably, the computational path delay of the Vedic multiplier is measured at 6.6 ns, indicating its remarkable speed.

The efficiency of the proposed MAC design, utilizing the 4x4 bit Vedic multiplier, surpasses that of conventional multipliers. This enhanced performance is particularly significant in applications where reducing time delays is imperative. The use of Vedic Multiplication technique proves highly suitable for achieving this objective. Furthermore, the innovative approach presented in this paper may pave the way for future research endeavors in this area, opening new avenues for exploration and advancement in high-speed computing architectures.

ACKNOWLEDGMENTS

I acknowledge with gratitude and humanity my indebtedness to Dr. Yogesh Suresh Angal, Professor and Head of Electronics and Telecommunication Department, BSIOTR, Wagholi, Maharashtra, India, under whose guidance and support I had the privilege tocomplete this work.

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