Performance Analysis of Double Gate JunctionlessTransistor For Mimicking Behaviour of BiologicalSynapse

Abhishek Verma
Dept. of ECE , (DoECE)
NIT Hamirpur
Hamirpur, INDIA

Vinod Kumar
Dept. of ECE , (DoECE)
NIT Hamirpur
Hamirpur, INDIA

***Abstract*—The use of a junctionless transistor with a charge trapping mechanism as a synthetic synaptic device for neuromorphic computing is highlighted in this paper.This work has examined and validated the long-term and short-term potentiation synaptic activities by storing the positive charges in the charge trapping nitride layer and floating body. Both band to band tunneling and impact ionization can be started by operating the junction-less device at a lower drain voltage V_{DS} = 1V. Comparing the channels made of silicon and silicon-germanium to perform the potentiation procedure.**

***Index Terms*—LTP, Neural Network, Junctionless, Charge Trapping Memory, STP, band to band tunneling, impact ionization.**

I. Introduction

A technique in computer engineering known as ”neuromorphic computing” models certain components of a computer after the nervous system and brain of a person. The phrase describes the architecture of a computing element’s hardware, which includes developing memory, as well as software, which handles signal transfer. It is also referred as neuromorphic engineering. Guided by principle of biological neural computation neuromorphic computing uses new algorithm approaches that emulates how human brain interact with world to deliver capabilities close to human cognition.

Overcoming Von Neumann computer’s limitations is a topic of major interest for neuromorphic computing [1]. Based on the von Neumann architecture, the modern computation architecture is implemented. The system performance is restricted by this architecture which transfers data in a linear series of calculation between the memory chips and the core CPU. There is a lot of interest in neuromorphic computing to address the shortcomings of Von Neumann computer[2].

An attempt has been made to construct highly integrated, energy-efficient electronic synapses for neuromorphic computing, emulating adaptive learning and memory in biological brain networks. Synapses, which connect neurons, are the basic units of neuromorphic structure in biological systems.

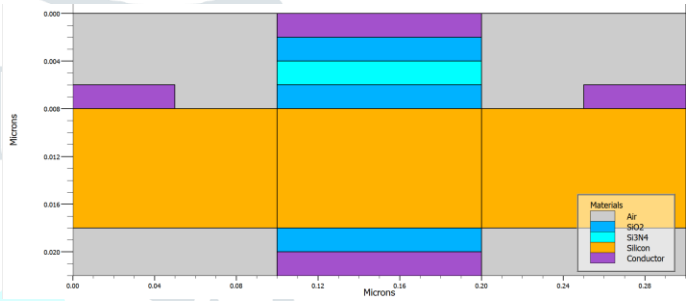

Fig. 1. Double Gate junctionless transistor with charge trapping machanism in silvaco using silicon as channel

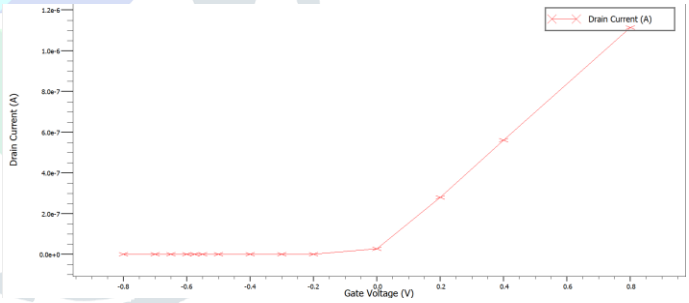

Fig. 2. VI characteristics of junctionless transistor with charge trapping mechanism in silvaco using silicon as channel

The synapses features such as Long term Potentiation:is the mechanism via which neurons synaptic connections get stronger with repeated activation. It is believed to be the process by which the brain adapts to experience, serving as the foundation for memory and learning. Long term depression:is the process via which a neuron’s synaptic connection weakens, long-term potentiation in opposition to a process[3]. Artificial synapses that use memristive devices are appealing because they mimic biological synapses and have the ability to adjust synaptic plasticity (strength).

However memristive devices have problems with repeata-

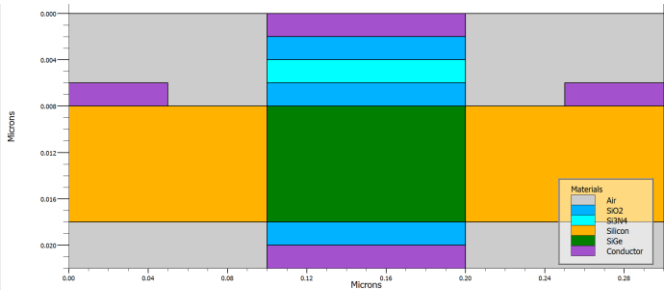

Fig. 3. Double Gate junctionless transistor with charge trapping machanism in silvaco using silicon-germanium as channel

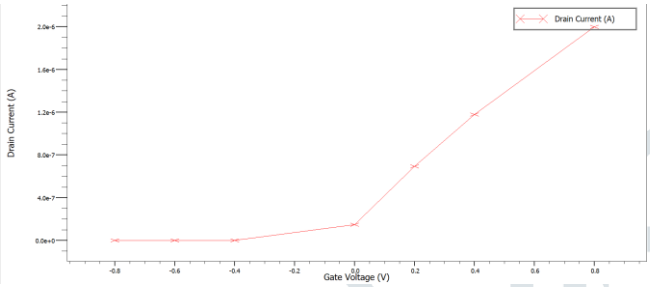

Fig. 4. VI characteristics of junctionless transistor with charge trapping mechanism in silvaco using silicon-germanium as channel

bility and low durability. Artificial synapses with memristive devices can modify the strength or plasticity of synaptic connections, exactly like biological synapses. Memristive devices suffer poor durability and repeatability issues. Since non-silicon components are used to construct these devices, co-integrating them with traditional complementary metal oxide semiconductor (CMOS) architecture presents a challenge. Short channel effect length scaling is a problem for conventional MOSFETs when it comes to high density and quick computation. These problems can be solved with a junctionless transistor that has the same doping type from the source to the drain.[4], [5].

In this study, we validate the synaptic properties (STP, LTP) of a junctionless (JL) transistor with a charge trapping mechanism. The ability to operate at a lower drain bias, which may result in ionization and band-to-band tunneling, is one advantage of the junctionless transistor. To assist the gadget use less power and energy, the potentiation operation is first carried out on the BTBT mechanism[7].

II. SIMULATION METHODOLOGY

Fig. 1 demonstrates the charge trapping memory mechanism (oxide/nitride/oxide) of a double gate n-type junctionless transistor for artifical synaptic device. The approach to obtain Non-volatile Memories with low operating voltage is to use SONOS structure. Semiconductor channels are produced with a thin layer of tunnel oxide, a thin layer of silicon nitride, a thicker oxide blocking layer, and a semiconductor polysilicon gate.The nitride-oxide band offset permits charge to build in nitride layers, and nitride contains trapping levels. In order to

Device Parameters	Value
Gate Length (L_g)	100nm
Silicon Channel depth (T_{Si})	10nm
Tunneling Oxide depth (T_{tox})	2nm (SiO_2)
Nitride Layer depth (T_{nox})	2nm (Si_3N_4)
Blocking Oxide depth (T_{nox})	2nm (SiO_2)
Oxide depth (T_{box})	2nm (SiO_2)
Gate 1 workfunction	p.polysilicon
Gate 2 workfunction	p.polysilicon
Channel doping (N_A)	10^{19} cm^{-3}
Source/Drain doping (N_D)	10^{20} cm^{-3}

TABLE I
DEVICE SPECIFICATION FOR SYNAPSE

accomplish low-voltage, low-power operation, direct tunneling charging requires an ultrathin tunneling layer[8].

The creation, recombination, trapping, and de-trapping of charges underpin the device's functioning as an artificial synapse. Non-local band-to-band tunneling (BTBT) and impact ionization models are used to simulate the charge creation and recombination in the silicon layer. Other models used are Concentration dependent SRH,field dependent mobility model , bandgap narrowing model for highly doped semiconductor film,and bipolar model for the silicon-on-insulator device are used[9]. For charge trapping and de-trapping, the Poole-Frankel and Fowler- Nordheim (F-N) models are combined with the dynamic dynasonos model. Table 1 shows how the device parameters were set up for the simulation. In order to exhaust the carriers from the device beneath the gate, a 100 nm gate length (Lg) and a 10 nm film thickness (TSi) are used to model the device. In this work, the front gate, also called Gate 1, is utilized as a charge-trapping memory consisting of an oxide, nitride, and oxide layer. Using the charge trapping memory, long-term depression and potentiation are seen. Using the charge trapping memory, long-term depression and potentiation are seen. In addition to demonstrating the behavior of short term potentiation and the transition from STP to LTP, the back gate aids in storing the holes in the floating body[2].

III. SIMULATION DISCUSSION

In this we have done comparision of silicon and silicon-germanium as channel in double gate junctionless transistor.

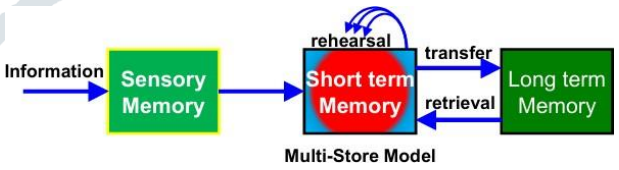

Fig. 5. Atkinson store model of the human brain[2]

Human memory is divided into three categories, according to the Atkinson Model of Memory Storage [1], which is seen in Fig. 5: sensory memory, short term memory, and long term memory. The sensory memory gathers data from its environment and temporarily stores it. Information gets transferred to STM if it is significant, else it is forgotten. The STM can store information for a little period of time,

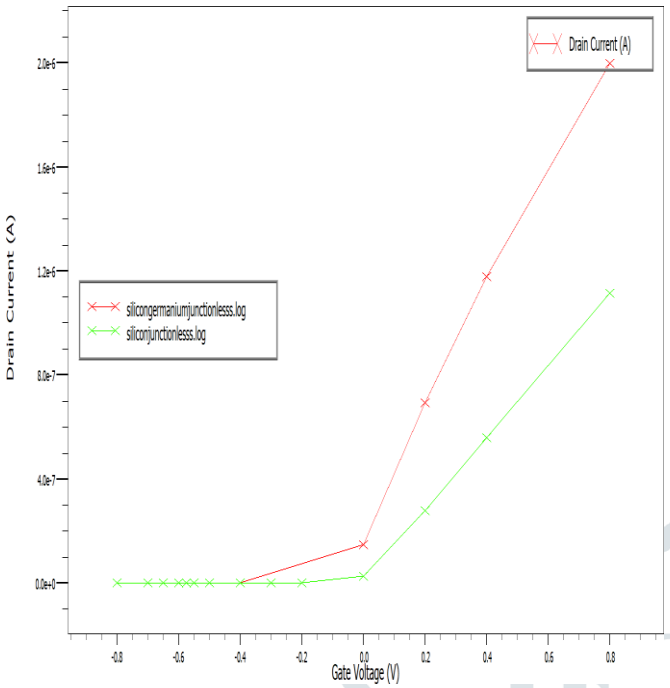

Fig. 6. Comparision between VI characteristics of junctionless transistor with charge trapping mechanism in silvaco using silicon and silicon-germanium as channel

Parameter	Silicon	Silicon-germanium
Ion	1.11291e-006	1.99695e-006
Ioff	2.68243e-008	1.47327e-007
vt	0.00615258 V	0.000247053 V
nsubvt	0.196698	0.297667
ratio Ion Ioff	41.4889	13.5545

TABLE II
COMPARISION BETWEEN DIFFERENT PARAMETER VALUE OF SILICON AND SILICON GERMANIUM

but if it is important, a rehearsal process is started. We may thus see the transition transitioning from STM to LTM. As a result, our goal is to artificially implement the Atkinson Model of hardware memory storage. Our suggested junction-less transistor technology uses synaptic learning, or potentiation (STP and LTP), to do this. In this experiment, a junctionless transistor mimics similar characteristics by applying a repeated stimulus. In this work, trapped charges in the nitride layer during potentiation and the transient analysis of a junctionless artificial synaptic device are demonstrated. For potentiation, a 50 ps pulse duration is used during the procedure. Obtain different Transient graph of potentiation operation using silicon and silicon-germanium as channel.From table2 can depict that silicon-germanium has better Ion as compare to silicon. Also see that silicon-germanium has higher Ioff has compare to silicon.Ioff tells us that there is leakage current in our device and that leakage current is not good for device because it degrades the retention capability of our device.

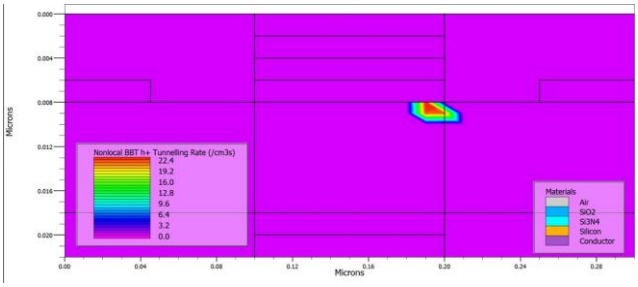

Fig. 7. Non-local Band to band tunneling in junctionless transistor

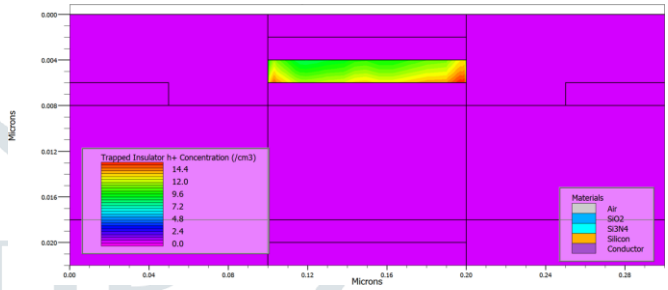

Fig. 8. Trapped holes in nitride layer in junctionless transistor

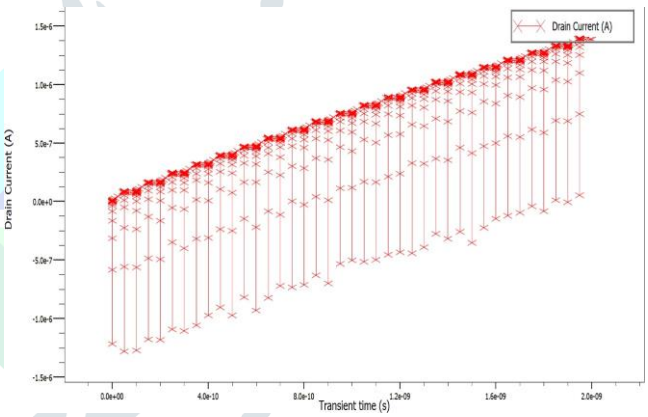

Fig. 9. Transient analysis in Juntionless transistor with silicon as channel during potentiation operation.

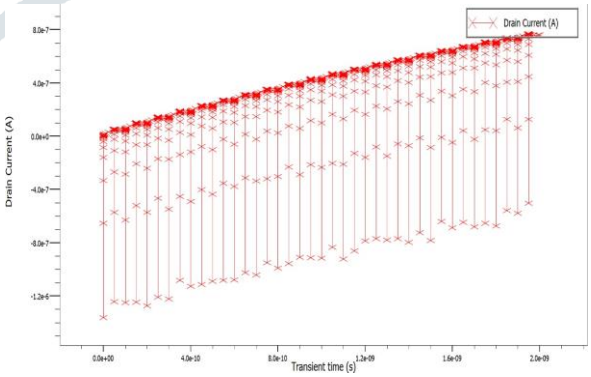

Fig. 10. Transient analysis in Juntionless transistor with silicon-germanium as channel during potentiation operation.

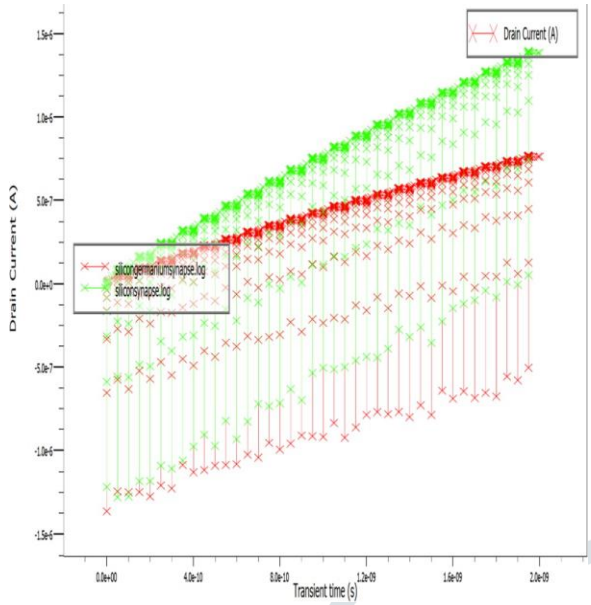

Fig. 11. Comparision of Transient analysis in Juntionless transistor with silicon and silicon-germanium as channel during potentiation

IV. CONCLUSION

We have shown that the junctionless transistor can function as a synthetic synapse in our work. The generation e-h pairs enable the conversion transitioning from STP to LTP. The junctionless-based technology has good image recognition accuracy, low power consumption, lower drain bias, and compatibility. Additionally, a comparison of silicon and silicon-germanium as a channel during potentiation operation reveals that the silicon-germanium has a worse retention capability than silicon due to a higher Ioff.

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