Performance Optimization of 14nm SOI-FinFETs Through Different Fin Materials

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***Abstract*—Silicon-on-insulator (SOI) FinFETs present notable benefits in terms of low power consumption and high performance when compared to traditional bulk FinFETs. This article investigates the optimization and performance evaluation of 14nm SOI FinFETs fabricated in Silvaco TCAD using a variety of channel materials (GaN, SiGe, GaAs, Si, and Ge). The study examines the effects of selecting the channel material and the dimensions of the device (including the thickness and height of the fins) on critical device parameters, including ion current, ioff current, ion/ioff ratio, threshold voltage, and subthreshold oscillation. The findings suggest that GaN FinFETs demonstrate enhanced ion current and an Ion/Ioff ratio in comparison to SiGe FinFETs, with comparable sub-threshold slopes of approximately 61.6 mV/decade. In addition, the research indicates that ion current is enhanced for both materials when the thickness of the fins is decreased.When utilized as a fin material, GaAs offers enhanced temperature controllability.**

***Index Terms*—SOI FinFET, Fin-Materials, Silvaco TCAD, Ion/Ioff ratio,sub-threshold slope,Temperature Controllability**

I. Introduction

The exponential increase in computing capacity and device integration density has been significantly propelled by the miniaturization of transistors, as predicted by Moore's Law [1] [2]. Nevertheless, the ability of traditional bulk CMOS technology to expand further is impeded by constraints such as heightened leakage currents and short-channel effects. Silicon-on-insulator (SOI) FinFETs have surfaced as a potentially viable substitute technology in order to surmount these constraints and present notable benefits for applications requiring low power and high performance [3].

This study investigates the optimization and performance evaluation of 14nm SOI FinFETs, expanding upon the well-documented advantages of this technology. According to the article referenced in the citation, SOI FinFETs provide enhanced electrostatic regulation, diminished parasitic capacitances, and superior scalability in contrast to bulk FinFETs. The aforementioned benefits can be ascribed to the distinctive three-dimensional configuration in which the channel is established on a slender silicon fin encircled by a bury oxide (BOX) insulating layer.

An investigation was conducted to further examine the performance optimization of SOI FinFETs through an analysis of the effects of different channel materials. These materials comprised gallium nitride (GaN), silicon germanium (SiGe), gallium arsenide (GaAs), silicon (Si), and germanium (Ge). Further investigation is conducted in this study to examine the impact of device dimensions (specifically, fin thickness and height) and channel material selection on critical device attributes. The aforementioned attributes comprise the on-current (Ion), off-current (Ioff), threshold voltage (Vt), sub-threshold swing (SS), and the ratio of Ion to Ioff (Ion/Ioff). Through the examination of these parameters, our objective is to ascertain the most effective configuration for low-power, high-performance SOI FinFET devices.

The effective channel breadth of an SOI FinFET is determined in part by the fin width (Wfin) and fin height (Hfin), both of which are critical design parameters. The equation delineated in reference [4] specifies the effective device width (W) in an SOI FinFET as follows:

$$W = 2 * Hf_{in} + Wf_{in}$$

In this context, the physical width of the fin is denoted by Wf_{in}, while the additional channel area exposed on the two sidewalls of the fin is accounted for by $2 Hf_{in}$. The desired device characteristics can be achieved by customizing the overall channel conductivity through the adjustment of the fin width and height.

The subsequent sections of this paper are organized as follows. In Section II, the device structure and parameters utilized in the design of the SOI FinFETs are described, emphasizing their prospective benefits and expanding upon the work referenced in [5]. The results and discussion, as well as the methodology utilized for device simulation and performance analysis, are detailed in Section III. This study aims to examine the influence of channel material and device dimensions on critical device attributes. In Section IV, the study's conclusions are outlined, and potential avenues for future research are examined.

II. Device Structure

By employing SiO2 as the buried oxide material and GaN for the fin, an SOI FinFET is simulated in Figure 1. A selection of the dimensions utilized in the SOI FinFET simulation are presented in Table 1 [6]. P-type impurities populate the

channel of the simulated device, while n-type impurities populate the source and discharge. GaN is employed in lieu of silicon due to its enhanced electron mobility and ability to conduct current. While it is recommended to perform moderate doping in the FinFET channel to enhance leakage current control, it is preferable to have the channel undoped or utilize FinFET technology [5]. As a result, the channel is doped to a magnitude of 1e16cm3. Conversely, significant contamination is present in both the source and outflow.

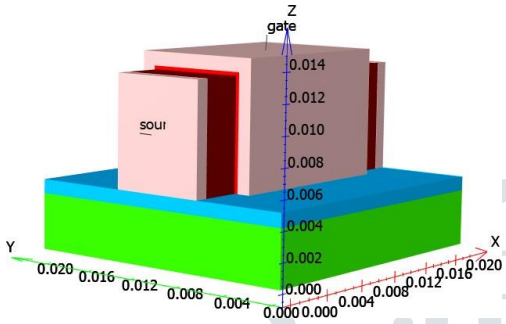

Fig. 1. 14 nm SOI-FinFET

TABLE 1 : DEVICE DESIGNING PARAMETERS

Fin height (H_fin)	8nm
Fin thickness (T_fin)	7nm
Fin width (W_fin)	3nm
Substrate thickness	4nm
Buried oxide thickness	1nm
Gate oxide thickness	0.25nm
Gate length	14nm
S/D doping concentration	1e20$cm^{-}3$
S/D doping concentration	1e16$cm^{-}3$

III. Results and Discussions

Simulations were utilized. In this study, we utilized SILVACO ATLAS TCAD [7], a 2D or 3D device simulator, to examine the electrical properties of SOI FinFETs featuring different channel materials. Our attention was specifically directed towards the leakage current behavior and transfer characteristics (Id vs Vgs), as illustrated in Figure 3. In contrast, the focus of our inquiry was on the effects of channel materials (specifically GaN, GaAS, SiGe, Si, and Ge) rather than gate oxide materials [8].

A. Relationship Between Channel Material and Transfer Characteristics in FinFETs

Expanding upon the well-documented advantages of high-K gate oxide materials in terms of enhanced channel control, the present investigation explored the impact of channel material choice on transfer characteristics. The findings of our research, which are depicted in figures not yet included in Fig. 2, indicate that FinFETs incorporating GaN channels outperform their SiGe, Si, and Ge counterparts. Particularly, GaN FinFETs demonstrate:

An increase in ion current (Ion) results in an enhanced capacity to conduct current in response to the application of the gate voltage (Vgs). Reduced leakage current (Ioff) signifies negligible current discharge during the off state, thereby enhancing the efficacy of the device. The previous findings can be assigned to the intrinsic material characteristics of GaN, including its greater electron mobility and broader bandgap in comparison to the alternative channel materials investigated [8]. A greater Ion concentration and reduced leakage result from the enhanced gate control over the channel made possible by the broader bandgap. Elevated electron mobility facilitates the acceleration of charge carrier motion, thereby augmenting the overall performance of the device.

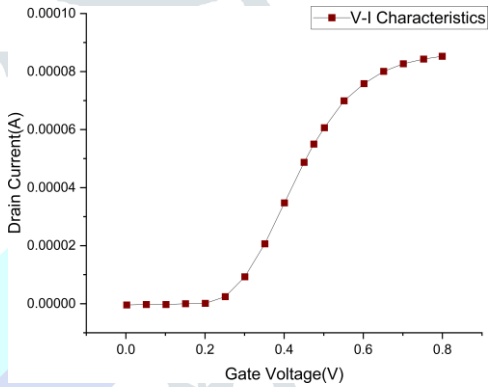

Fig. 2. SOI-FinFET's Transfer characteristics with Gan as a Fin material

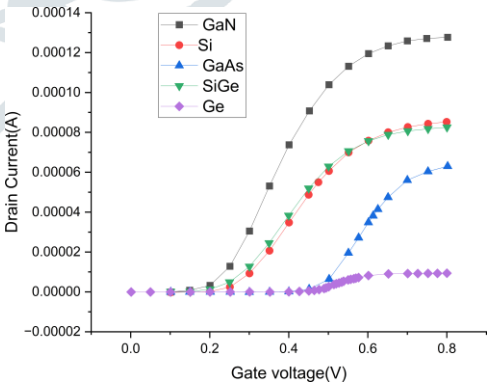

Fig. 3. SOI-FinFET's Transfer characteristics using different fin materials

B. Temperature-Dependent Characterization

Silicon-on-Insulator (SOI) FinFETs' electrical characteristics are notably altered by an increase in temperature [9]. This segment delves into the aforementioned effects, with a specific emphasis on the impact of different channel materials, namely GaN, GaAs, SiGe, Si, and Ge. An increase in temperature causes the subsequent modifications in SOI FinFETs: Reduced Ion On-Current (Ion): Elevated temperatures not only promote the mobility of carriers but also amplify carrier scattering, resulting in an overall reduction in the conductivity of the ion.

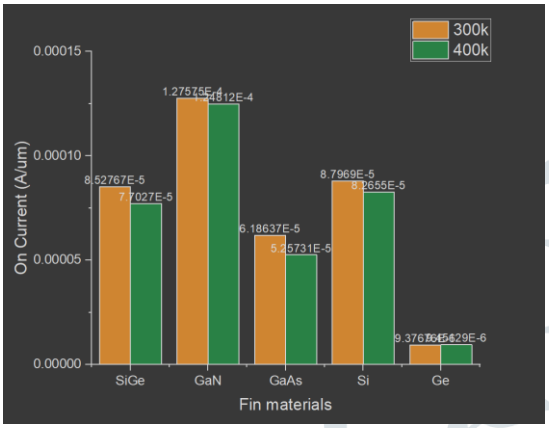

Fig. 4. On current at 300k and 400k using different fin materials

Elevated Off-Current (Ioff): The increase in temperature induces a greater quantity of excited carriers, which subsequently leads to a heightened leakage current (Ioff) in the off state. Reduced Threshold Voltage (Vt): The threshold voltage (Vt) necessary to activate the device decreases as a result of thermal effects that erode the gate's control over the channel. Elevated subthreshold slope (SS): As temperatures rise, the abruptness of the transition from the on to off states diminishes, manifesting as an increased subthreshold slope (SS). Impact of Channel Content:

The primary objective of this study was to determine the effect of 300K and 400K temperature on SOI FinFETs comprised of various channel materials (GaN, SiGe, Si, and Ge). The results depicted in Figure 4 indicate that the channel material has a distinct effect on temperature sensitivity:

GaN exhibits the maximum ion values (12.7 mA/um) and ioff value (27.8 nA/um) at both temperatures in comparison to the other materials. This suggests that GaN FinFETs exhibit enhanced current conductivity, particularly when operating at elevated temperatures of 400K.GaN exhibits a significantly broader bandgap in comparison to the aforementioned materials [8], [9]. At elevated temperatures, a greater bandgap corresponds to a reduced quantity of free carriers that are excited by thermal energy. By decreasing the dispersal of conduction electrons, the overall on-current is increased.

Compared to SiGe, GaAs provides superior temperature regulation; however, it has a lower drive current (Ion). This phenomenon could potentially be attributed to the higher thermal conductivity of GaAs in comparison to SiGe. Although GaAs may undergo a marginal reduction in Ion as a result of enhanced scattering, its increase in leakage current (Ioff) at elevated temperatures is expected to be more restrained in comparison to SiGe.

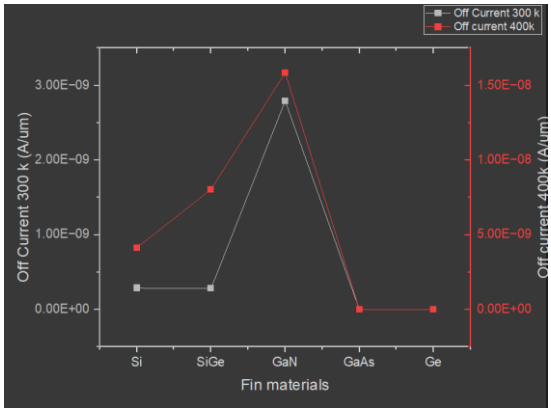

Fig. 5. Off current at 300k and 400k using different fin materials

C. Analysis of Threshold Voltage and Subthreshold Regime in FinFETs

The influence of channel material selection on the subthreshold slope (SS) and threshold voltage (Vt) of SOI FinFETs is the subject of ongoing research. A range of channel materials, including GaN, GaAs, SiGe, Si, and Ge, were utilized in order to compare their Vt and SS properties.The findings indicate potential variations in Vt among various materials.

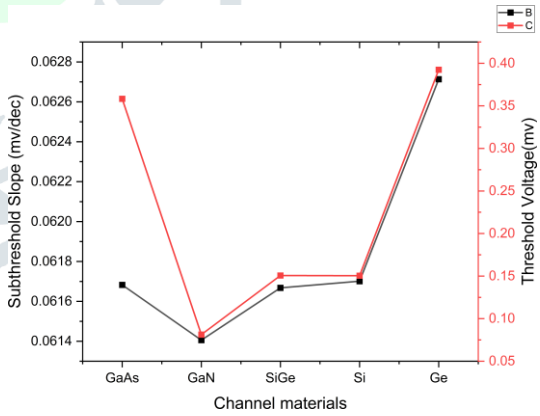

Fig. 6. Threshold voltage and subthreshold characteristics

Furthermore, the data points may suggest that certain channel materials, potentially GaN, attain subthreshold slope values (61.4 mV/decade) that are more in line with the optimal value of 60 mV/decade than others [10]. This study contributes to the body of research that investigates the impact of gate oxide materials on Vt and SS, thereby offering significant knowledge regarding the selection of channel materials to enhance the performance of SOI FinFETs [2].

CONCLUSION

The objective of this research project was to enhance the effectiveness of 14nm SOI FinFETs by examining the effects of channel material choice and temperature. Expanding upon the reference paper's illustration of the advantages attributed to high-K gate oxide materials in terms of enhanced channel control, our study investigated the effects of channel materials (GaN, GaAs, SiGe, Si, and Ge) on electrical properties. In contrast to other materials that were examined, GaN FinFETs demonstrate superior performance, according to the findings. GaN provides: Enhanced regulation of leakage current (Ioff) results in a reduction in off-state current and an increase in overall efficiency. Enhanced temperature regulation: The increased bandgap of GaAs mitigates the adverse consequences of elevated temperatures on carrier mobility and leakage current. Although GaN exhibits exceptional performance, it may possess a reduced drive current (Ion) in comparison to certain materials such as SiGe. This compromise between leakage and drive current must be taken into account in accordance with particular application specifications.

Additionally, the analysis underscores the adverse effects that temperature has on the efficacy of SOI FinFETs. Temperature increases are typically accompanied by a reduction in on-current (Ion), an increase in off-current (Ioff), a decrease in threshold voltage (Vt), and an increase in subthreshold slope (SS).

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