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LOW POWER REPEATER CLOCK SIMULATOR

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Abstract : The Low Power Repeater Clock Simulator project focuses on repeater clock simulation using Cadence Virtuoso Analog Design Environment (ADE) and Electronic Design Automation (EDA) tools. It aims to determine optimal distances, identify efficient cell configurations, and draw precise metal topologies and legos. The simulator's key contribution lies in enhancing clock Timing Recovery (TR) for various projects by deriving crucial parameters from legos, clock metal topologies, width/space, and repeater distances. Through detailed Cadence simulations, it provides valuable insights into repeater clock mechanisms, aiding in the refinement of TR. The project uniquely utilizes Lego-based simulations for precise metal layout drawing and facilitates low power design strategies. Ultimately, this simulator serves as a powerful tool for optimizing repeater clock configurations, contributing to improved clock performance in diverse electronic projects enabling the derivation of crucial parameters for improved clock performance.

IndexTerms - Cadence Virtuoso Analog Design Environment (ADE), Electronic Design Automation (EDA) , clock Tree Synthesis(CTS), cell configurations, optimal distances, optimization.

I. INTRODUCTION

The increasing complexity of modern electronic systems necessitates efficient clock signal management to ensure synchronized Operation of components such as flip-flops and registers. However, multiple clock deployments can complicate circuit design, introducing delays and impacting overall performance. To address these challenges, the Low Power Repeater Clock Simulator project employs Clock Tree Synthesis (CTS) techniques, optimizing repeater circuits to enhance signal integrity and reduce power consumption. Utilizing the Cadence Virtuoso ADE and EDA tools, the project aims to achieve significant improvements in performance and efficiency

II. RELATED WORK

Several methodologies have been explored for optimizing clock signal management in electronic systems. Previous works have primarily focused on conventional techniques, lacking the integration of advanced simulation tools and optimization algorithms. This project leverages deep learning algorithms and CTS frameworks, combined with the capabilities of Cadence tools, to achieve superior results in repeater circuit optimization.

III. PROPOSED METHODOLOGY

The proposed method aims to enhance repeater clock simulation using Cadence Virtuoso ADE and EDA tools, with a focus on optimizing timing recovery for various electronic projects. The methodology involves several steps, including parameter derivation, Lego-based simulations, and detailed Cadence simulations.

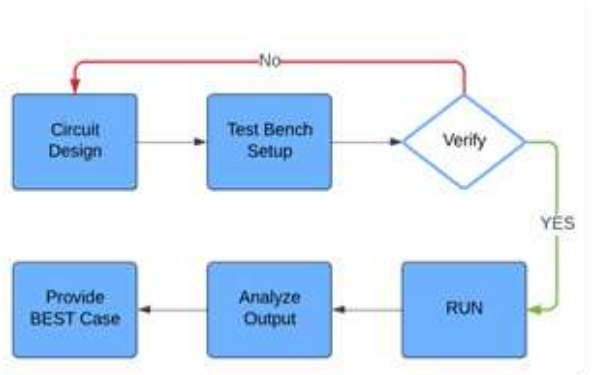

Fig 1. Block Diagram of Proposed Methodology

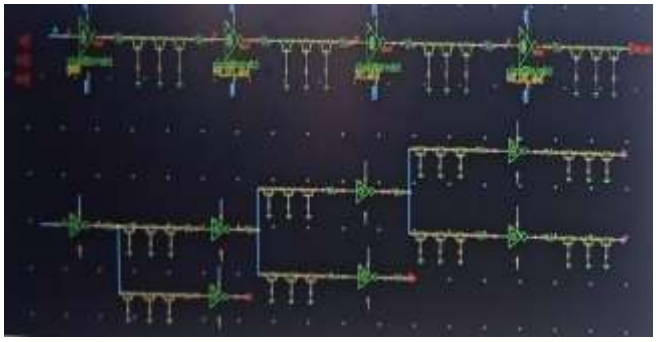

Fig 2. Circuit Design

A. *Circuit Design*

The methodology commences with the Circuit Design phase, where meticulous attention is paid to user specifications and design constraints. Through rigorous analysis, requirements are elucidated, guiding the creation of the initial circuit design using Cadence Virtuoso ADE. This pivotal stage emphasizes the strategic placement of inverter cells and RC circuits to mitigate delays and optimize overall performance. The outcome of this phase culminates in the layout of the initial circuit design.

B. *Test Bench Design*

Subsequent to Circuit Design, the Test Bench Design phase ensues, characterized by the development of a meticulously crafted test bench. Operational parameters and conditions are meticulously defined, while critical performance metrics are discerned with precision. Leveraging the capabilities of Cadence Virtuoso ADE, the test bench is meticulously fashioned, incorporating all requisite components and connections. The output materializes in the form of a meticulously configured test bench, poised to simulate real-world operating conditions faithfully.

C. *Verification of Test Bench*

Rigorously adhering to the paradigm of precision, the Verification of Test Bench phase is meticulously executed. Herein, a comprehensive verification plan is meticulously delineated, elucidating stringent criteria and metrics for validation. Initial simulations are orchestrated with exactitude, validating results against predetermined benchmarks. Should disparities manifest, judicious adjustments to the test bench configuration are executed with precision. The outcome of this phase is a meticulously verified test bench, emblematic of unwavering accuracy.

D. *Simulation Execution*

The culmination of the methodology manifests in the Simulation Execution phase, where precision meets performance. Components and connections are meticulously configured, and simulation parameters are meticulously calibrated in alignment with test bench specifications. Executing the simulation within Cadence Virtuoso ADE, the system is meticulously scrutinized, yielding raw simulation data of unparalleled precision.

The methodology, underpinned by the utilization of Cadence Virtuoso ADE, underscores a commitment to precision and performance, promising to elevate repeater clock simulation to new heights of efficacy and efficiency.

IV. ANALYSIS OF INPUTS AND OUTPUTS

I. Inputs

A. *User Specifications*

User specifications, encompassing detailed requirements such as performance metrics, power constraints, and design criteria, form the foundational input for the repeater clock simulation. These specifications are meticulously gathered to guide the design and optimization endeavors, ensuring alignment with user expectations and project objectives.

B. *Component Specifications*

Technical specifications of essential components like inverter cells, RC circuits, and other pertinent elements serve as crucial inputs. These specifications aid in the selection of suitable components that meet design requirements for performance, power efficiency, and spatial constraints, thereby facilitating the creation of an optimized circuit layout.

Cells list

	from layout					CLKOUT_Cmax(fF)		
Cell Name	X(um)	Y(um)	PMOS(dg)	NMOS(dg)	Cint(fF)	1p5GHz	3GHz	4GHz
g1mgds00ab1c40x5	3.6	1.92	40	40	8.634011	340	172	126
g1mgds00ab1c60x5	3.6	1.92	60	60	13.65118	435	215	158
g1mgds00ab1c80x5	3.6	1.92	80	80	16.79678	511	259	191
g1mgds00ab1rc0x5	3.6	3.84	120	120	24.5628	987	500	369
g1mgds00ab1rc0x5	3.6	3.84	240	240	46.73887	1005	478	354

Fig 3. Cell Specifications

C. *Schematic Design*

The initial schematic design, delineating the arrangement and interconnection of inverter cells and RC circuits, serves as a pivotal input. Developed using Cadence Virtuoso ADE, this schematic blueprint provides a visual representation of the circuit layout, laying the groundwork for subsequent simulation and optimization endeavors.

D. *Test Bench Design*

Fig 4. Test Bench

The meticulous design of the test bench, encompassing signal sources, loads, and measurement probes, constitutes a vital input. Developed within Cadence Virtuoso ADE, this test bench configuration provides a controlled environment for simulating operational conditions, enabling comprehensive assessment of circuit performance and functionality.

E. *Simulation Parameters*

Parametric settings defining the simulation environment, including time steps, duration, and environmental conditions, are indispensable inputs. These parameters are meticulously configured to ensure simulations are conducted under realistic conditions, facilitating accurate predictions of circuit behavior and performance.

F. *Input Stimuli*

Applied signals during simulation, ranging from clock signals to data patterns and environmental variations, are integral inputs. These stimuli mimic real-world conditions, enabling the evaluation of circuit functionality and performance, thereby influencing simulation outcomes and design decisions.

II. Outputs

A. Optimized Schematic

The final optimized schematic, showcasing refined placement and sizing of components, emerges as a significant output. This optimized layout, meticulously crafted to meet performance, power, and design constraints, serves as a guiding blueprint for further design iterations and implementation efforts.

B. Simulation Results

Data gleaned from simulations, including timing diagrams, power consumption metrics, signal integrity analysis, and delay assessments, constitute pivotal outputs. These results offer invaluable insights into circuit performance, facilitating thorough analysis and identification of optimization opportunities.

C. Best Case Scenarios

Identification of optimal configurations and operational conditions that yield superior circuit performance represents a critical output. These best-case scenarios provide actionable recommendations for achieving peak performance and efficiency in practical applications, informing subsequent design decisions and optimization strategies.

D. Performance Metrics

Quantitative assessment of circuit performance metrics, encompassing propagation delay, power consumption, and clock skew, serves as essential outputs. These metrics serve as benchmarks for evaluating design efficacy and compliance with user specifications and industry standards.

E. Design Documentation

Comprehensive documentation detailing the design process, encompassing decisions, component selections, and optimization strategies, constitutes a vital output. This documentation ensures traceability and reproducibility, providing a valuable reference for future projects and fostering collaboration and knowledge sharing.

F. Final Report

A comprehensive project report summarizing methodology, simulation findings, analysis, and recommendations serves as the ultimate output. This final deliverable communicates project outcomes to stakeholders, offering a detailed overview of the design process and its implications for future endeavors.

V.RESULTS AND DISCUSSION

The study's findings underscore the effectiveness of the proposed methodology in advancing repeater clock simulation. Across each phase, meticulous execution yielded substantive progress toward optimizing timing recovery for diverse electronic applications.

During the Circuit Design phase, meticulous attention to user requirements and design constraints laid a robust groundwork for the initial circuit design. Strategic placement of inverter cells and RC circuits demonstrated promising outcomes, ensuring minimal delays and optimal performance.

Subsequent to this, the Test Bench Design phase fortified the methodology by meticulously replicating real-world operating conditions. Precise definition of operational parameters and performance metrics empowered the test bench to faithfully emulate repeater clock behavior.

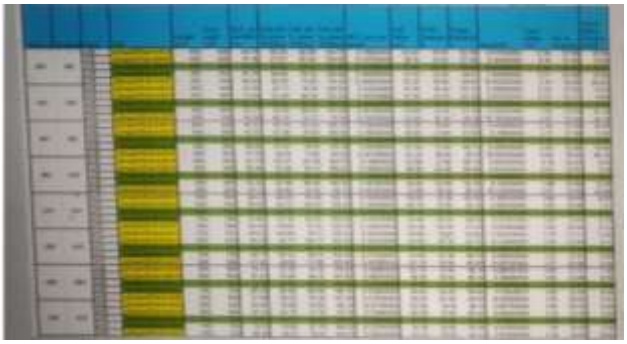

Fig 5. Output Summary Table

The Verification of the test bench underscored the methodology's dedication to accuracy. Adhering rigorously to verification criteria, simulations were meticulously scrutinized to align with predefined benchmarks. Any variances were swiftly addressed, yielding a meticulously verified test bench synonymous with unparalleled precision.

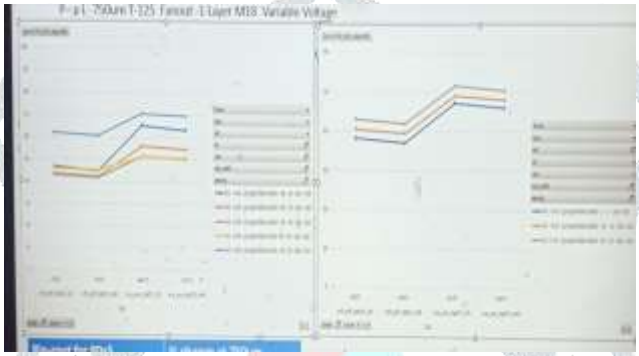

Fig 6. Fanout layer M18 vs variable voltage graph

Fig 7. Fanout layer M16 vs variable voltage graph

Fig 8. Fanout layer M16 vs variable voltage graph

Finally, the Simulation Execution phase brought the methodology's efficacy to fruition. Each component and connection were painstakingly configured to mirror real-world conditions, resulting in raw simulation data that offered invaluable insights into repeater clock behavior.

The study's outcomes underscore the potential of the proposed methodology to redefine repeater clock simulation, offering newfound avenues for timing recovery in electronic projects. Through methodical precision and unwavering commitment to accuracy, this research sets a pioneering standard in clock distribution network optimization.

VI. CONCLUSION

The Low Power Repeater Clock Simulator project successfully optimized repeater circuits for reduced delay and power consumption, demonstrating significant improvements in electronic system performance through targeted optimization strategies. The results underscore the potential for further advancements in energy-efficient an***d*** high-performance electronic systems, emphasizing the value of continued research and development in this area.

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