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A Low-Power and High-Accuracy Computing Technique using 4:2 Approximate Compressor

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Abstract: The aim of the paper is to design approximate multiplier by designing an approximate compressor with high accuracy compared to existing approximate compressors. For applications that have error tolerance, employing an appropriate multiplier is an emerging method to reduce critical path delay and power consumption. An appropriate multiplier can trade off accuracy for lower energy and higher performance. In this paper, we not only propose an approximate 4:2 compressor with high accuracy, but also an adjustable approximate multiplier that can dynamically truncate partial products to achieve variable accuracy requirements. The proposed approximate multiplier can adjust the accuracy and power required for multiplications at run-time based on the users' requirement.

Index Terms **- Approximate compressor, 4:2 compressor.**

I. INTRODUCTION

Multipliers, being fundamental components in digital circuits, play a critical role in executing complex multiplication operations, forming the backbone of numerous computational task. In any conventional multiplier, there are three basic stages like Generation of partial product, Reduction of Partial product and addition of propagated carries of previous stage. Compressor circuits are energy efficient and used for adding the partial product elements of the high performance multipliers. In this paper, we propose an innovative approach to designing approximate multipliers by incorporating approximate in multiplier designs, and introducing approximate adders offers an intriguing opportunity to enhance the overall efficiency of multipliers. The primary objective of this research is to explore and evaluate different approximate multiplier designs, each integrating approximate adders, in a comparative manner. We seek to answer critical questions regarding the trade-offs between accuracy, speed, and power efficiency. Multipliers are extensively used in digital signal processing where the speed of multiplication and area of power consumption are important. The objective of optimal multiplier is to provide low power consumption and high speed. If appropriate optimized multiplier is not chosen it ultimately produces lag in digital circuits.

Multiplication plays an important role in order to carry out the operations in Digital filters, DSP, image processing, etc. The primary block performing such operations are known as multipliers, which consume more power and operating time. In any conventional multiplier, there are three basic stages like Generation of partial product, Reduction of Partial product and Addition of propagated carries of previous stage. Partial product reduction is very complicated while using compressors. The functionality of compressor is to count the number of ones in the given input. Also, these are the fundamental processing elements (PEs) for the collection of partial products in the multiplication operation. Compressors provide knowledge regarding the progressive increasing demand of reduced power and high speed in the overall critical path of the circuit.

II. RELATED WORK

An Approximate computing is widely used to have energy-efficient system design in Very Large-Scale Integration (VLSI). This approach is best suited for signal processing and multimedia applications where low power consumption is the main concern. Faster and significant results can be obtained from an approximate computing at the cost of reduced accuracy. In this work, we proposed a very novel design approaches based on various monolithic compressors. Proposed approach is applied to have reduced stages in the partial product multiplication. Proposed Monolithic compressor had outperformed over various 4:2 compressors. Our proposed method is based on majority logic based with the use of Dadda multiplication. Compressors calculate the sum and carry at each stage simultaneously. The resultant carry is added with a higher significant sum bit in the next level. This process is continued until the final product is produced.

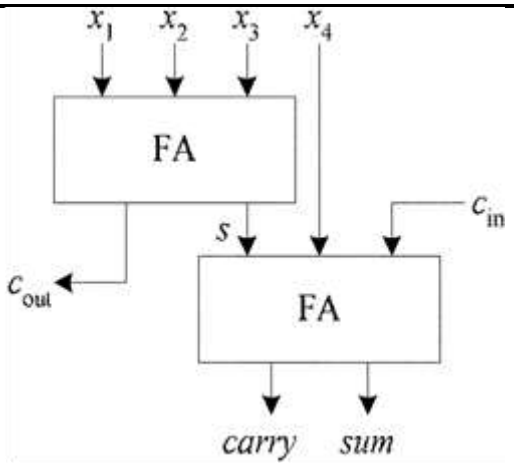

Fig. 1 The Full Adder based 4-2 Compressor Design

III. PROPOSED METHODOLOGY

Many high end surveillance and medical applications based on image and video processing algorithms need high reliability and most important utmost precision. But on other hand there many arithmetic logic based processing algorithms in which human visibility it seems to be accurate though it remains numerically approximate. The numerically inaccurate results provides some freedom of relaxation to proceed with an approximate computation. This kind of requirement give the new era of research idea that incorporates low-power designs with reduced area and less propagation delay in different abstraction levels. In this paper we try to propose the new approximate arithmetic computing based approach for the Dadda.

In initial stages of multiplier we have proposed an approximate adder i.e. Almost full adder based adder compressor and later stages we have proposed majority logic based hybrid combination for Dadda multiplier design. In this paper we try to propose the new approximate arithmetic computing based approach for the Dadda. In initial stages of multiplier we have proposed an approximate adder i.e. Almost full adder based adder compressor and later stages we have proposed majority logic based hybrid combination for Dadda multiplier design. This approach has given consequence reduction in the output delay. Majority logic based approach suffice the problem of the above mentioned all 4:2 compressors having AND- OR and XOR combination. Proposed approach will reduce the circuit latency and hardware complexity at the cost of exploiting more negligible error.

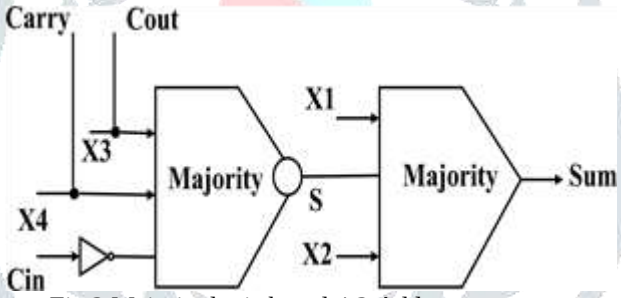

Fig.2 Majority logic based 4:2 Adder compressor

IV. IMPLEMENTATION

Xilinx Tools is a suite of software tools used for the design of digital circuits implemented using Xilinx Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD). In this paper, we propose an innovative approach to designing approximate multipliers by incorporating approximate in multiplier designs, and introducing approximate adders offers an intriguing opportunity to enhance the overall efficiency of multiplier. The primary objective of this research is to explore and evaluate different approximate multiplier designs, each integrating approximate adders, in a comparative manner. We seek to answer critical questions regarding the trade-offs between accuracy, speed, and power efficiency.

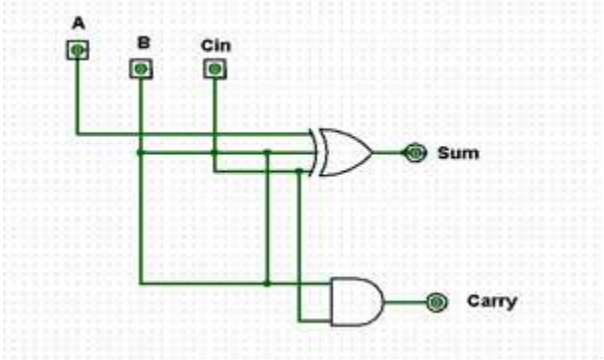

Fig. 3 Proposed almost full adder

The Verilog source code template generated shows the module name, the list of ports and also the declarations (input/output) for each port. Combinational logic code can be added to the verilog code after the declarations and before the endmodule line. Xilinx Tools can be started by clicking on the Project Navigator Icon on the Windows desktop. This should open up the Project Navigator window on your screen. You can create a Verilog HDL input file(.v file) using the HDL Editor available in the Xilinx ISE Tools (or any text editor). In the previous window, click on the NEW SOURCE. Select Verilog Module and in the “File Name:” area, enter the name of the Verilog source

file you are going to create. Also make sure that the option Add to project is selected so that the source need not be added to the project again. Then click on Next to accept the entries.

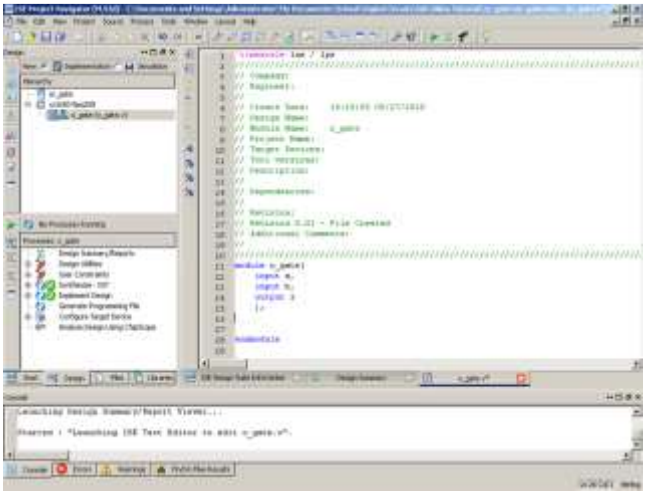

Fig. 4 Verilog Source code editor window in the Project Navigator (from Xilinx ISE software)

The design has to be synthesized and implemented before it can be checked for correctness, by running functional simulation or downloaded onto the prototyping board.

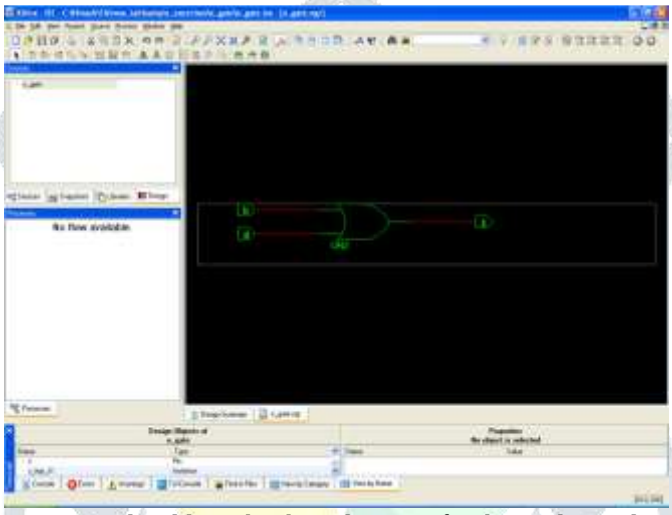

Fig.5 Realized logic by the Xilinx ISE for the verilog code

Abbreviations and Acronyms

DSP – Digital Signal Processing, PE – Processing Elements, VLSI – Very Larg Scale Integration, FPGA – Field Programmable GateArray, CPLD – Complex Programmable Logic Devices, ISE – Integrated Synthesis Environment.

4.1 Population and Sample

Now a days Dadda multiplier is employed for high-speed multipliers. The design approaches use 4:2 and 5:2 compresses; which reduces the partial product stages for multiplication. Accurate array multiplier fall out in terms of speed compared to 8×8 bit broken Dadda multiplier Error recovery modules could also be realized by utilizing 4:2 approximate compressors with achieving a reduction in hardware part, more accuracy and low power consumption.

Apart from this, in case of faulty rows incompressor truth's table, input to the compressor can be encoded to achieve reduction in error rate by employing partial product reduction tree.

4.2 Data and Sources of Data

A.Momeni, J. Han, P. Montuschi, and F. Lombardi, "Design and analysis of approximate compressors for multiplication," IEEE Trans. Comput., vol. 64, no. 4, pp. 984–994, Apr. 2015. Inexact (or approximate) computing is an attractive paradigm for digital processing at nanometric scales. Inexact computing is particularly interesting for computer arithmetic designs. This paper deals with the analysis and design of two new approximate 4-2 compressors for utilization in a multiplier.[2]

M. H. Moaiyeri, F. Sabetzadeh, and S. Angizi, "An efficient majoritybased compressor for approximate computing in the nano era," Microsyst. Technol., vol. 24, no. 3, pp. 1589–1601, Mar. 2018. Approximate computing is an effective paradigm for energy-efficient hardware design in nanoscale. In this study, an efficient 4:2 compressor for approximate computing in the nano era is proposed.[3]

4.3 Theoretical Framework

The novelty approach for error resilient image and signal processing applications have been designed with approximate compressors. The significant reductions in area and power with high signal to noise ratio were the achievements as results in these kind of algorithms. In this paper the new approximate arithmetic computing based approach for the Dadda is proposed. In initial stages of multiplier an approximate adder is proposed i.e. Almost full adder based adder compressor and later stages majority logic based hybrid combination for Dadda multiplier design is proposed.

The moderate digital design logic with less power consumption and minimal de- vice utilization are the two main objectives of this implementation proposed in this paper, which maintains the performance nearly same as exact multiplication process. In this paper, also proposed a novel design approach based on majority 4:2 compressor is also proposed to have reduction in partial product stage of multiplication.

This approach has given consequence reduction in the output delay. Section II describes brief overview of proposed almost full adder and majority logic based adder. Different 4:2 compressors designed with almost full adder based and majority logic based approaches. Partial product reduction analysis in Dadda multiplier with combination of almost full adder based 4:2 compressor and majority based full adder design. Section V demon- strated simulation results followed by conclusion.

Equations

Majority logic-based approach suffice the problem of the above mentioned all 4:2 compressors having AND- OR and XOR combination. Proposed approach willreduce the circuit latency and hardware complexity at the cost of exploiting more negligible error. Consider Table 1 for the truth table of almost full adder, comparing with accurate almost full adder.

Table 4.1: Truth table of one bit accurate and proposed almost full adder

Inputs			Conventional Full Adder		Almost Full Adder	
A	**B**	**C**	**Sum**	**Carry**	**Sum**	**Carry**
0	0	0	0	0	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	1	0	0	1	0	0
1	1	1	1	1	1	1

$$\text{Sum} = A \wedge B \wedge C \quad (1a)$$

$$\text{Carry} = BC \quad (1b)$$

$$C_{out} = (x1 \oplus x2) \cdot x3 + x1 \cdot x = (x1 \oplus x2) \cdot x3 + (x1 \oplus x2) \cdot x1 \quad (2)$$

$$S = (x1 \oplus x2 \oplus x3 \quad (3a)$$

$$sum = (S \oplus x4 \oplus C_{in}) = (x1 \oplus 2 \oplus x3 \oplus x4 \oplus C_{in}) \quad (3b)$$

$$Carry = (S \oplus x4) \cdot C_{in} + S \cdot x4 = (x1 \oplus 2 \oplus x3 \oplus x4) \cdot C_{in} + x1 \oplus 2 \oplus x3 \cdot x4 \quad (3c)$$

$$S = \text{Maj}(X1,X2,X3) \quad (4a)$$

$$\text{Carry} = X4 \quad (4b)$$

$$\text{Sum} = \text{Cin} \quad (4c)$$

V. RESULTS AND DISCUSSION

5.1 Input and output Values of Exact and Approximate Multipliers

Table 5.1: Comparison Table

INPUTS	EXACT MULTIPLIER OUPUTS	APPROXIMATE MULTIPLIER OUTPUTS
A = 255, B = 225	O/P = 65025	O/P = 63408
A = 8, B = 3	O/P = 24	O/P = 32
A = 15, B = 15	O/P = 255	O/P = 212
A = 15, B = 14	O/P = 210	O/P = 122
A = 12, B= 15	O/P = 180	O/P = 80
A = 12, B = 12	O/P = 144	O/P = 96

Table 5.1 shows that approximate multiplier introduced minor errors, which were acceptable for error-tolerant applications, low enough to maintain high perceived quality in applications like image processing and minimal visual quality degradation in multimedia applications, indicating high practical utility despite approximations. Table 5.1 shows that exact multiplier has zero errors, providing exact results which are necessary for applications requiring high precision, such as scientific computations.The comparison between the 4:2 approximate compressor and the exact multiplier revealed significant advantages in power and area efficiency for the approximate design. Future advancements could further enhance the utility and performance of approximate compressors, especially in system-level implementations.

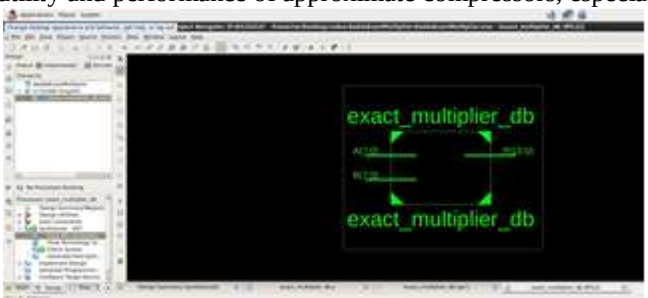

Fig. 6 RTL Schematic Diagram of 8-bit Multiplier

The RTL (Register-Transfer Level) schematic analysis provided insights into the structural and functional differences between these designs, emphasizing power efficiency and accuracy.

Fig.7 Simulation Results of Approximate Multiplier

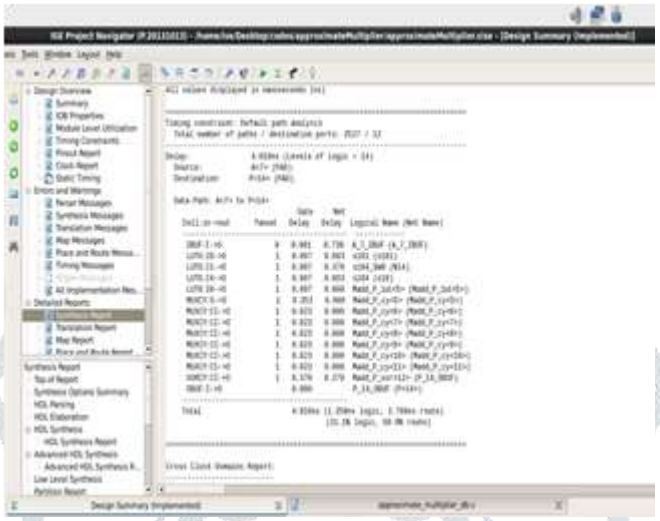

Fig.8 Total Delay in Approximate Multiplier

The reduced critical path delay results in faster processing speeds and lower latency, enhancing performance in real-time applications. It can be seen in Fig. 5.4 that while there is a trade-off between power savings and accuracy, the approximate compressor achieves a good balance, offering significant power and area savings with minimal impact on accuracy for error-tolerant applications. The approximate compressor is ideal for applications where minor errors are acceptable, such as image and video processing, machine learning inference, and certain signal processing tasks while for applications requiring high precision, such as scientific computations or financial calculations, the exact multiplier remains the preferred choice due to its accuracy.

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