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# POWER EFFICIENT 8T SRAM CELL DESIGN USING CHARGE SHARING TECHNIQUE

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***Abstract:*** The aim of the paper is to design and analyze 8T SRAM Cell using Charge Sharing Technique where a standard 8T SRAM cell performance degrades with low power supplies. In the design the SRAM cell uses a charge sharing technique between the transistors to make SRAM more rigid against noises that occur due to low power supplies. Apart from noise reduction the read discharge power is reused. The comparison between standard 6T, 8T and 8T with charge sharing is made. It shows that less power consumed by 8T with charge sharing than others. charge power is reused. The comparison between standard 6T, 8T and 8T with charge sharing is made. It shows that less power consumed by 8T with charge sharing than others.

***Keywords-6T SRAM***

## I. INTRODUCTION

A basic low power SRAM cell is designed by using cross-coupled CMOS inverters with 6 transistors giving basic 6T SRAM cell. However, with technology scaling below nanometer the power dissipation of 6T SRAM Bbecomes significant with low power supplies as due to this the gate delay is increased which reduces the frequency of operations. Due to growing demand of portable battery-operated embedded systems made a necessity for energy efficient design. As predicted 90 % of systems will be made up of memory and the memory management is need of the time. The SRAM is popular choice for embedded systems for its high speed, robustness and ability easy to manufacture.

## II. RELATED WORK

It is noteworthy that for associate SRAM cell, the specified form of operation is commonly set with the correct choice of the bit line voltage. However, this involves additional edge circuits like bit line precharge circuits and writes drivers to create positive correct bit line voltage setting before any operation. At low provide voltages due the soundness limitations of 6T SRAM cell we tend to use 8T SRAM cell for quick transmission applications. it's like 6T SRAM cell with a scan decoupled path that consists of M5 and M6 transistors. Allow us to see the operating of 8T SRAM style.

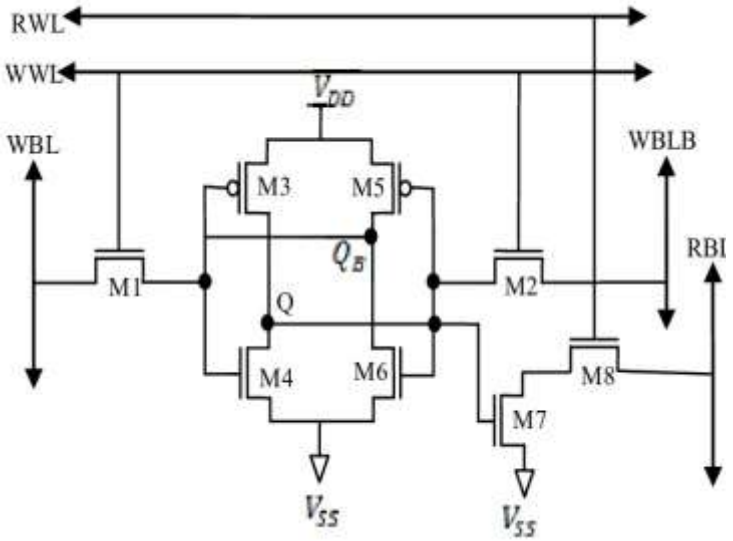



Fig 1 8T SRAM

## III. PROPOSED METHODOLOGY

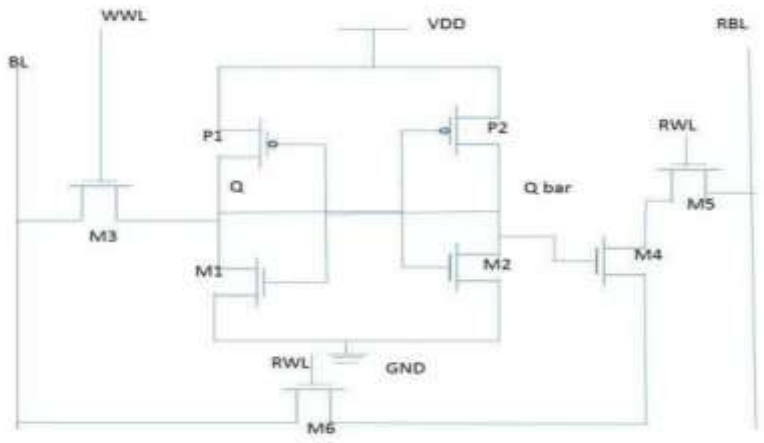



Fig 2 Design of Low power Memory Architecture using 10t SRAM Driver

Here the proposed SRAM design is using the concept of charge sharing of 10T SRAM design. But the difference is that the design is done with less number of transistors when compared to the above 10T SRAM which also decreases the area of the design and in the proposed design we also reduced the power consumption when compared with the previous design. The proposed SRAM consists of a single ended 7T bit cell which has one bit line (BL) for write operation and one Read Bit cell for read operation.During the write operation WWL was enabled and RWL was disabled (i.e RWL='0') so M4 M5 M6 are in the off state. The cell acts like single ended 5T SRAM Cell and writes the Bit line data into the cross coupled inverter pair P1 M3 and P2 M2.

During the read operation the bit line disconnected from inverter pair because of WWL='0' during read phase and RWL was enabled so M6 M5 will be in the ON state. For read operation here we are using separate bit line called RBL instead of using same BL. SO during read operation RBL was PR recharged. Read '0': In reading '0' M4 was ON state, so RBL has a discharging path from M4 M5 and M6, the M6 will acts like a charge sharing network, instead of discharging the charge to the ground M6 will charge the bit line (BL) so there will no loss of power to the ground. Read'1': In reading '1' M4 was OFF state so there will be no discharging path for RBL to discharge maintains the charge and reads the '1'.

## IV IMPLEMENTATION

### Digital Circuit Design Using Tanner S-Edit Tools

### S Interface and Setup

S-Edit is a fully hierarchical computer-aided schematic capture application for the logical design of integrated circuits. S-Edit contains integrated SPICE simulation and probing of simulation results, including voltages, currents, and noise parameters.

### Launching S-Edit

To launch S-Edit, double-click on the S-Edit icon.


The user interface consists of the elements shown below. Unless you explicitly retrieve a setup file, the position, docking status and other display characteristics are saved with a design and will be restored when the design is loaded.

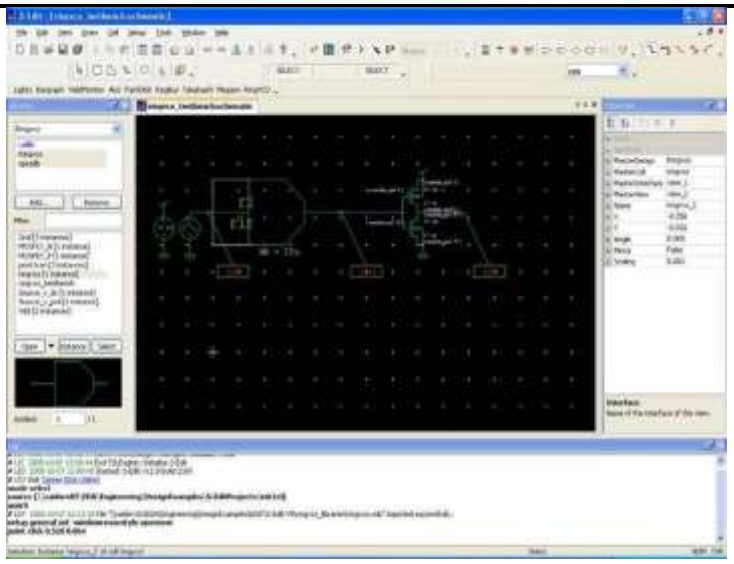


Fig 3 Interface

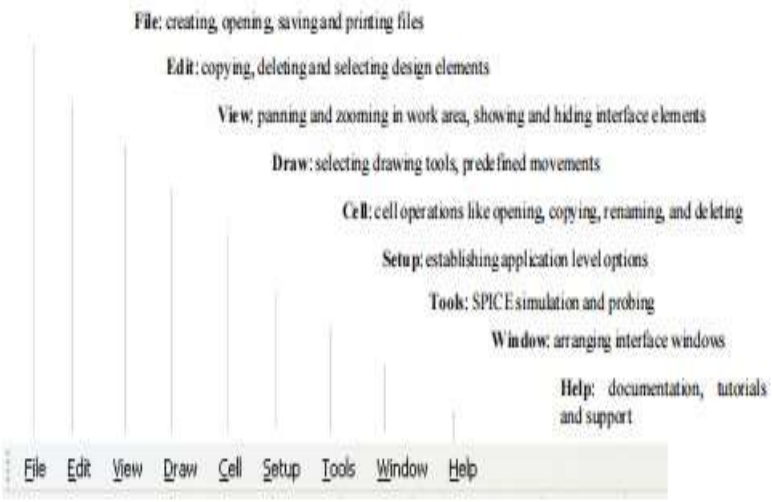
**Parts of the Interface**

**Title Bar**

The *title bar* shows the name of the current cell and the view type (symbol, schematic, etc.).

**Menu Bar**

The *menu bar* contains the S-Edit menu titles. The menu Displayed may vary depending on the view type that is active. See Shortcuts for Cell and View Commands for the various methods S-Edit provides for executing commands




***MenuListFiltering:***

Most S-Edit menus and dialogs allow for filtering to speed the process of selecting from a drop-down list. So, when you enter a character, S-Edit will jump to the first list item that begins with that character. For example, typing g highlights the first list item beginning with that letter and filters the display to show only items that begin with g. Typing a u after the g highlights the first list item beginning with gu, and filtersthe display to show only items that begin with gu, and so on

**Toolbars:**

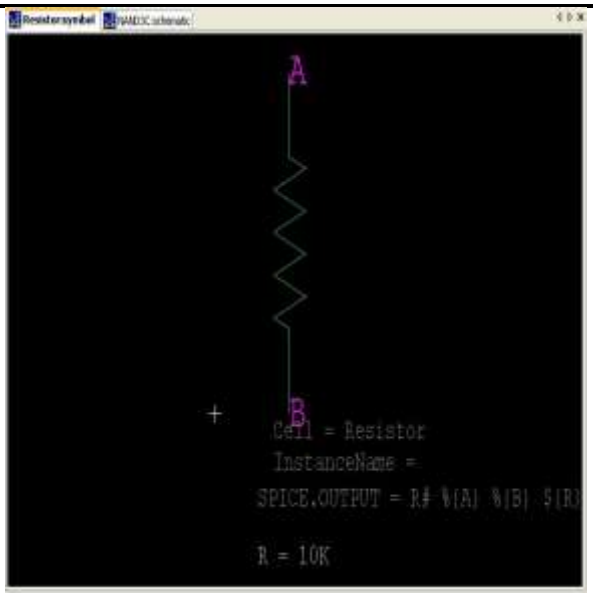
You can display or hide individual toolbars using the **View > Toolbars** command, or by right-clicking in the toolbar region.Toolbars can be relocated and docked as you like. For added convenience, S-Edit displays a tool tip when the cursor hovers over an icon.

***Toolbar Options:***

This drop-down menu lets you add or remove buttons from the S-Edit toolbars

**Design Area**

The design region in Tanner tools, where you create, viewand edit objects, is the *Design Area*. The portion of the.design area currently visible is called the *Work Area*.




**Edit Project File Structure**

S-Edit stores design information in several different files in the {*designname*} directory.
**design.edif** is the design itself.
**design.old.edif** is a backup of the design that is overwritten each time the design is saved.
**{*designname*}.tanner** is the TCL file that launches a design. It specifies the path, cell, and windows to open, and references the other three files
**dockinglayout.xml** stores any previously used (or else the default) workspace settings
**libraries.list** references the libraries used in the design. Library path names can be edited if desired.
**edit.lck** is a file that prevents an open design from being opened elsewhere.The **setup** folder stores any changes that have been saved from the Setup dialog

## V RESULTS AND DISCUSSION

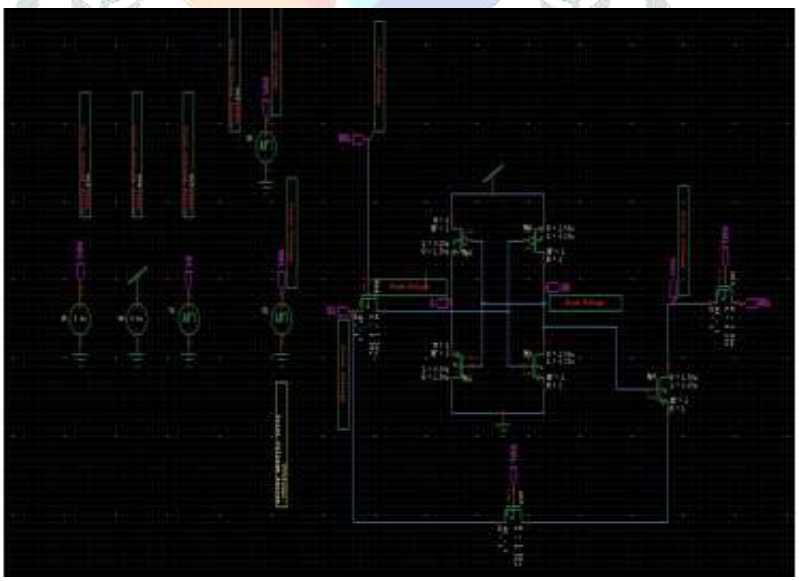


Fig 4 PROPOSED SRAM CIRCUIT

Fig 5 Final Simulation

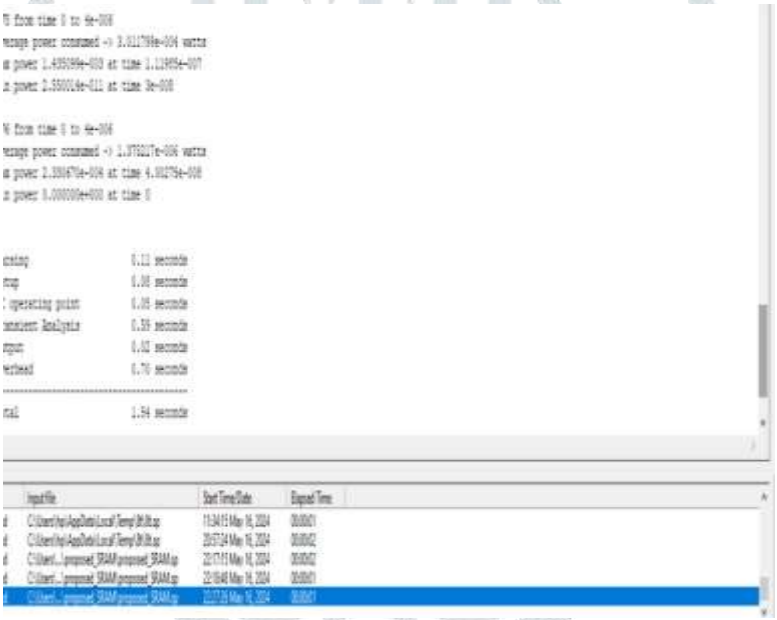


Fig 6 Power Consumption

## VI CONCLUSION

We have implemented the design of SRAM utilizing charge-sharing techniques and conducted an analysis to optimize for minimum area and power consumption. This design approach not only reduces power but also ensures robust stability levels compared to traditional 6T and 8T SRAM cell designs.

## VII.REFERENCES

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