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A Quantum Cost Efficient Reversible MultiplexerFor Low Power Applications

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Abstract— *Low power architectures are more pronounced for different applications that extend from Internet of Things to Quantum computing. Primitive combinational logic circuits induce from bit deletion due to information loss during the processing of input information which results in energy loss. The computations involving reversibility cancel the loss of information by sustaining the input bits from output. In the basic arithmetic and logic units, the combinational circuits play a significant role in determining the performance of the processor. The principles involved in the design of reversibility is an upcoming technology for ultra-low power applications. The reversible logic circuits furnish a thoroughly new way to progress in Quantum computing. In this article, we propose an energy tolerant low power reversible multiplexer with optimum energy loss. The proposed multiplexer also reduces the ancillae, garbage outputs and quantum cost considerably.*

Keywords— Quantum computing, bit erasure, energy loss, processor, reversibility.

I. INTRODUCTION

The rapid increase in the need for digital devices to meet human day-to-day needs has significantly raised the proportion of information handled by these devices. Consequently, the number of devices required to process this immense volume of information has grown over time. Although the dimensions of these devices have shrunk to accommodate more components on integrated circuits, this miniaturization faces physical limits. A critical issue in traditional computing is heat dissipation, which hinders development because of the irreversible nature of primitive computing. Information loss during operations results in energy dissipation, quantified by Landauer's principle as (KT ln 2) Joules per bit at a temperature of 300 K, amounting to \(2.9 \times 10^{-21} \) Joules. While this energy loss seems negligible now, it poses a significant barrier as technology scales down.
Reversible computing offers a solution to the limitations of traditional computing. As demonstrated by R. Landauer and further explored by Bennett, reversible computing can ideally achieve zero energy dissipation by using bijective functions, making information lossless circuits. This
potential to drastically reduce or even eliminate energy dissipation has spurred interest in reversible computing. Applications in nano computers, cryptography, and digital processing further enhance its appeal, making it a crucial research area.
Quantum computing, which uses qubits as units of information, represents a shift from classical bits. Qubits can exist in multiple states simultaneously, unlike the definite 0 or 1 states of classical bits. This superposition requires reversible gates for operations since traditional gates, which transform multiple bits into a single output bit, cannot handle the parallel states of qubits. Reversible gates enable the retrieval of input states and allow computations to move backward. Quantum computing, with its reversible nature, holds promise for next- generation applications such as stock market prediction and weather forecasting.

This paper proposes a low-power, reversible multiplexer designed to minimize energy loss and reduce ancillae, trash outputs, and quantum cost. The paper is organized into four sections for a comprehensive performance comparison. Section II covers the basic principles of reversible logic gates. Section III presents the performance evaluation of the proposed multiplexer. Finally, SectionIV concludes the finding.

II. RELATED WORK

Logic gates to a greater extent in primitive computation are not reversible. The relation between the outputs and the inputs in primitive logic gates is not bijective but it is many to one [14]. Consequently, the relation between the output and the input in terms of reversible gates is bijective i.e. one-to-one. In precise, a primitive function, K, maps the inputs and the outputs as K: Lx →Ly, where x, y are the positive numbers and L takes only two logic values. For instant a two input OR gate has only one output with two inputs [15]. Now let us consider a logic function in reversible case as, K, which maps the inputs and the outputs as K: Lx →Lx,

where x is a positive integer and L takes two values, with the bijective function being obeyed In this case, the number of inputs and number of outputs are the same as shown in Fig.1

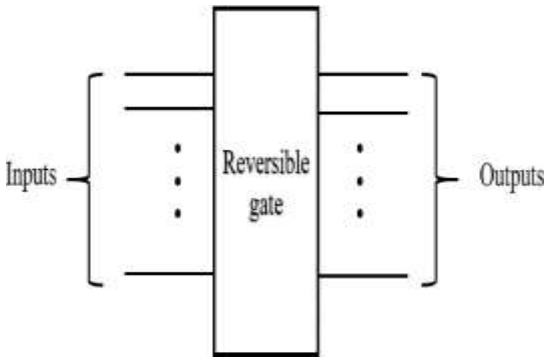

Fig1.REVERSIBLE GATE

Here always a distinct output is produced from the distinct input. In case of n-variable Boolean reversible function, the truth table needs 2n columns and 2^n rows. Let usconsider a NOT gate as shown in Table.II. By seeing the truth table, it generates a distinct output for each distinct input, thegate is reversible.

For an irreversible gate to transform to a reversible gate, we need to include either extra inputs or outputs depending on the requirement. The extra inputs which we addto make the irreversible gate into a reversible gate are called ancillae [19]. The extra outputs which we obtain to make an irreversible gate to a reversible gate are called are garbage outputs.

The primitive computation maps manifold inputs to a beneath output. A truth table gives a comfortable way to relate the outputs and the inputs. Let us consider the truth table of two input OR gate.

TABLE I. TRUTHTABLE OF PRIMITIVE OR GATE

Inputs		Outputs
0	0	0
0	1	1
1	0	1
1	1	1

From truth table, it can be seen that the input and the output relation is not one-to-one. Thus, the states of input cannot be found by checking the states of output. The output values from the truth table are 1 for the distinct states of inputs(0,1), (1,0) and (1,1). By checking the output value as1, we cannot find the inputs as (0,1), (1,0) and (1,1). This shows that for primitive logic gates, the relation is not bijective [16]. With the exception in primitive logic gates that only NOT gate produces bijective functions i.e. one-to-one and onto.

TABLE II. TRUTHTABLE OF NOTGATE

Input	Output
0	1
1	0

Some common reversible gates used in combinational circuits are:

A. Feynman gate

It is the basic reversible gate. Also called as Controlled NOT gate. It is 2 X 2 logic gate with 2 inputs and2 outputs. This reversible gate can be used either to pass (buffer) or to invert the input signal. In most of the applications, the Feynman gate is used when fan out isrequired. Thus this gate is also called as Fan-out gate.

TABLE III.TRUTH TABLE OF FEYNMAN GATE

Inputs		Outputs	
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

B. Toffoli Gate

Toffoli gate is also 3 X 3 reversible gate with 3 inputs and3 outputs. It is also called as Controlled NOT gate[16]. In general, it is formed by cascading of Feynman gates.

TABLE IV. TRUTH TABLE OF TOFFOLI GATE

Input			Output		
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

C. Cog gate

Cog gate is also known as New Fredkin gate. The Cog gate is formed by cascading of Feynman gate and Fredkin gate. The operation of cog gate is almost similar to that of Fredkin gate. In case of Fredkin gate, it generates only one Swapping operation of the control inputs. Whereas in Cog gate, it generates the two Swap operation of all the control inputs. In case of all 3 input 3 output reversible gates, the minimum quantum cost is attained by cog gate.

Table V. Truth Table of Cog Gate

Inputs			**Outputs**		
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	0	1
1	1	0	1	0	0
1	1	1	1	1	1

I. PROPOSED SYSTEM

The design of proposed multiplexer is done in three stages. Initially the most significant bit of selection lines is considered with least significant two input bits to generate the partial output expression. The desired output in first stage is used as selection line in the second stage. In second stage the most significant two input bits are considered. Finally, the output is generated in the third stage where the least significant bit of the selection line is considered and generated the output.

The same selection lines, s1 & s0 are applied to both 4x1 Multiplexers. The data inputs of upper 4x1 Multiplexer are I7 to I4 and the data inputs of lower 4x1 Multiplexer are I3 to I0. Therefore, each 4x1 Multiplexer produces an output based on the values of selection lines, s1 & s0.

The outputs of first stage 4x1 Multiplexers are applied as inputs of 2x1 Multiplexer that is present in second stage. The other selection line, s2 is applied to 2x1 Multiplexer.

If s2 is zero, then the output of 2x1 Multiplexer will be one of the 4 inputs I3 to I0 based on the values of selection lines s1 & s0.

If s2 is one, then the output of 2x1 Multiplexer will be one of the 4 inputs I7 to I4 based on the values of selection lines s1 & s0.

Therefore, the overall combination of two 4x1 Multiplexers and one 2x1 Multiplexer performs as one 8x1 Multiplexer.

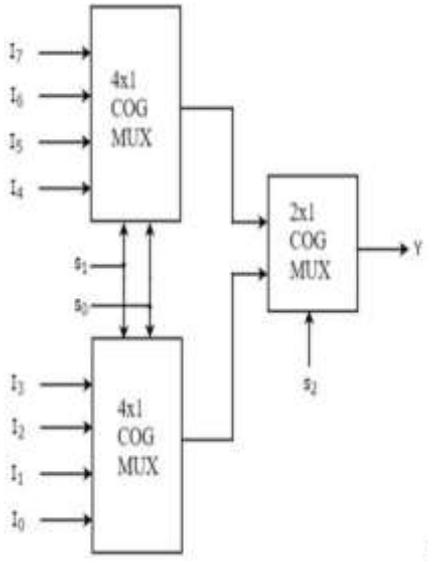

FIG 2. PROPOSED DESIGN OF 8X1 MULTIPLEXER

The output expression for the proposed multiplexer is

$$Y = S'_0S'_1S'_2 I_0 + S'_0S'_1S_2I_4 + S'_0S_1S'_2I_1 + S'_0S_1S_2I_5 + S_0S'_1S'_2I_2 + S_0S'_1S_2I_6 + S_0S_1S'_2I_3 + S_0S_1S_2I_7$$

II. RESULTS

The simulation results of an 8x1 COG (Control Output Gate) multiplexer provide insights into how the circuitbehaves under different conditions, such as varying input combinations and control signals.

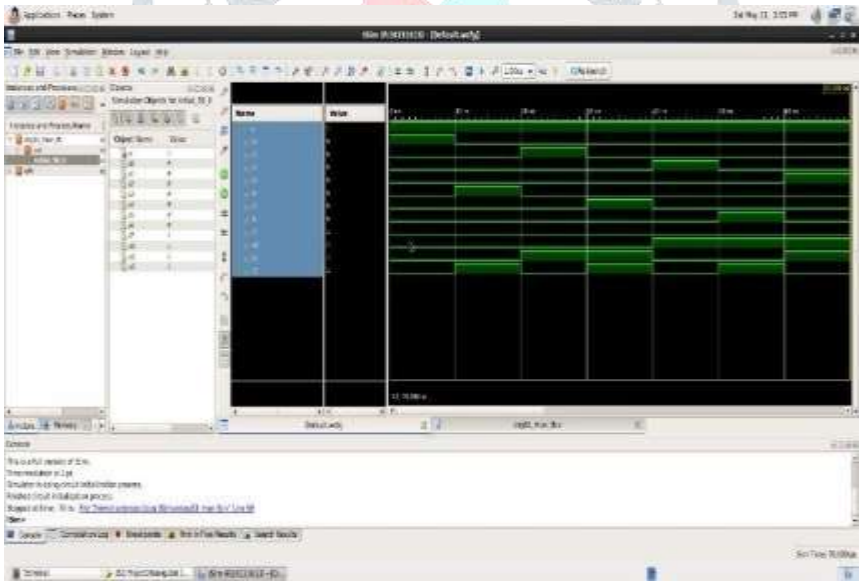

Fig 3. Simulation results of 8x1COG Mux

The simulation results will likely include informationabout the input signals provided to the multiplexer. This includes the values of the eight data inputs (I0 to I7) and the control signals used to select one of the inputs as the output.

The primary focus of the simulation results will be on the output signal of the multiplexer. It will show the value of the output signal corresponding to the selected input based on the control signals. This allows us to verify that the multiplexer correctly selects and outputs the desired data input.

There will be 3 select lines for 8 input lines. Among the 8 input lines one of the input line is selected as the output

The select lines combination are from 0 (s0=0, s1=0, s2=0) to 7(s0=1, s1=1,s2=1)

The simulation results may include waveforms showing the behavior of the output signal over time. These waveforms provide a visual representation of how the output signal changes in response to changes in the input signals and control signals. They can help identify any timing issues or glitches in the output signal.

III. CONCLUSION AND FUTURE SCOPE

An efficient design of multiplexer is proposed in this article for ultra-low quantum cost and ultra-low power applications. As the primitive logic gates dissipate heat energy, the reversible gates form the basic need for modern computing. The multiplexers are very widely used in VLSI and communication environment. Thus a new design of multiplexer is proposed where the main parameters of focus is quantum cost. There is a reduction of 25% of quantum cost of proposed multiplexer than the existing multiplexer architectures. Thus the proposed multiplexer is much pronounced to quantum cost.

The future scope of quantum cost-efficient reversible multiplexers for low power applications is quite promising. Reversible logic, which is the foundation of these multiplexers, is gaining attention due to its potential to reduce power consumption significantly. This is particularly important as the industry moves towards nanoscale technologies where power dissipation becomes a critical concern.

Here are some key points regarding the future scope:

It's a promising direction for emerging technologies that may replace or enhance traditional computer chip efficiency1. Reversible logic gates allow for computations where the inputs can be recovered from the outputs, which is crucial for quantum computing and low power CMOS applications1.

Reversible logic circuits inherently minimize energy dissipation, which is crucial for sustainable computing. As energy efficiency becomes increasingly important in electronics and computing, reversible multiplexers can play a significant role in reducing power consumption in various applications.

The design of low power fault-tolerant reversible multiplexers is a step towards low power, nano-scale circuit design for future generation quantum computers3.

In summary, the development of quantum cost-efficient reversible multiplexers is expected to play a crucial role in the advancement of low power applications, quantum computing, and nanotechnology. The research in this field is ongoing, and anticipation can more efficient designs with lower quantum costs and power consumption in the near future.

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