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A Efficient Approximate Vedic Multiplier: Design, Analysis, and Application in Image

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Abstract: Approximate computing has become a widely recognized method for designing energy efficient arithmetic architectures in the context of error-tolerant applications. This paper presents the design and analysis of a 4-bit approximate Vedic multiplier (AVMT) using the Urdhva Tiryagbhyam method. This Vedic approach, involving vertical and crosswise steps, outperforms traditional multiplication in terms of efficiency. An approximate 2-bit multiplier (AVM2) is designed, and an AVMT is proposed using AVM2. The proposed architecture has better propagation delay and less area utilization compared to other conventional multipliers. AVMT has an 11% reduction in area consumption and a 12% increase in processing speed compared to the exact Vedic multiplier. To assess its practicality in real-world scenarios, the proposed multiplier is integrated into an image-blending application. The results indicate that the system achieves a Structural Similarity Index (SSIM) average value of 0.91, which proves to be suitable for error-resilient image processing applications.

Index Terms - Vedic Multiplier, Approximate Computing, Image-Blending

I. INTRODUCTION

In the realm of modern computing, there is an incessant demand for high-speed and energy-efficient arithmetic operations to support an array of applications, ranging from signal processing to image manipulation. Multipliers, being fundamental components in digital circuits, play a critical role in executing complex multiplication operations, forming the backbone of numerous computational tasks. Traditional multipliers are designed for precise and accurate computations, but they often come at the expense of increased hardware complexity, power, and processing time. As the focus shifts towards optimizing these factors to meet the demands of contemporary computing systems, researchers have explored alternative methodologies that embrace the concept of approximate computing. Approximate computing offers a unique trade-off between computational accuracy and efficiency [1]. It allows for the relaxation of strict precision requirements, thereby Mathematics to perform multiplication operations efficiently. By leveraging techniques like Nikhilam Sutra (specifically UrdhvaTiryagbhyam) and Ekadhikena Purvena, the Vedic multiplier reduces the number of required operations, leading to minimized hardware resources and improved computational speed compared to conventional multipliers

This paper deals with the design of approximate Vedic multiplier using hardware enabling the design of specialized hardware architectures that prioritize speed and reduced hardware utilization [2-3]. Numerous methods for multiplication have been devised to enhance the efficiency of the multiplier, addressing both algorithmic and structural aspects. These methods address the minimization of partial products and their subsequent addition, yet the fundamental principle of multiplication remains consistent across all scenarios. One unique approach is the "VEDIC" (Vedic Mathematics) multiplier, which draws inspiration from ancient Indian mathematical techniques. The Vedic multiplier employs a novel algorithm that exploits the principles of Vedic reduction approximation technique to make it energy-efficient for error-tolerant application. A 4-bit approximate multiplier (AVMT) is proposed

with help of 2-bit approximate multiplier (AVM2). AVMT has better electrical hardware performance compared other conventional multipliers. An imageblending application is employed to assess the effectiveness of the proposed AVMT.The remainder of this paper is organized as follows: Section II delves into the methodology and design principles behind the proposed AVMT. Section III presents a thorough evaluation of the multiplier's performance, including comparisons with conventional multipliers. In Section IV, we detail the integration of the proposed multiplier into an image blending application, showcasing its efficacy and suitability for realworld image processing tasks. Finally, Section V concludes the paper.

II. PROPOSED APPROXIMATE VEDIC MULTIPLIER

In this section, the Urdhva-Tiryakbhyam sutra based, an AVM2 is designed with the help of an approximate adder. Finally, AVMT is proposed.

A. Urdhva-Tiryakbhyam

AVM2is designed using Urdhva-Tiryakbhyam vedic mathematics sutra and the multiplication operation is shown in Fig.1.

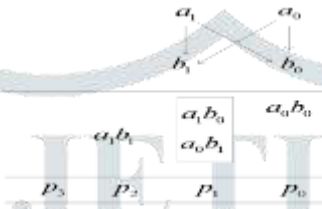

Fig. 1. Vedic Multiplication

The term "Urdhva Tiryakbhyam" can be translated as "Vertically and crosswise" in English. This method is a key approach employed in Vedic Mathematics for achieving speedy and effective multiplication [5-7]. Consider the multiplicand and multiplier to be two-bit binary values, a_1a_0, and b_1b_0, respectively. In this method, the multiplication process starts by vertically multiplying the least significant bits of two numbers (a_0, b_0), namely the multiplicand and the multiplier and the result is p_0. Subsequently, a cross-wise multiplication occurs between the a_0 and b_1. The result of this multiplication is added to the product obtained from multiplying the b_0 and a_1. This combined result provides the second bit (p_1) of the final product along with a carry bit (c_1). Continuing the process, the a_1 and b1 are multiplied vertically. This operation yields the third bit (p_2) of the final product, accompanied by another carry bit (c_2) that is fourth bit (p_3) of the final product [8-11].

B. Design 2×2 Approximate Vedic Multiplier

Two approximate half adders and four partial product generators are used to design AVM2 that is shown in Fig.2. Final results are four bits and these are $p_3p_2p_1p_0$.

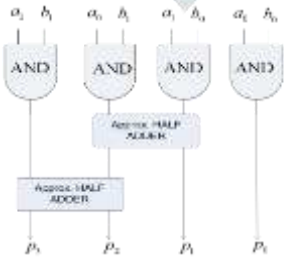

Fig. 2. Block Diagram of AVM2

The exact and approximate half-adder truth table is shown in Table.1. In exact half-adder sum is calculated by XOR of A and B. This XOR logic is approximated by the OR gate therefore an error of -1 is produced for input A=1 and B=1 with probability 1/9. The logical expression of an approximate half-adder is defined by equations 1 and 2.

$$S_{app} = A+B \quad (1)$$

$$C_{app} = A.B \quad (2)$$

This AVM2 is useful for the design of energy efficient architecture at a cost of tolerable error. The 2-bit approximate multiplier design uses an approximate half adder, to sum up partial products that make it energy efficient.

TABLE I. HALF ADDER AND APPROXIMATE HALF ADDER

A	B	S=A⊕ B	C=A.B	S_{app}=A+B	C_{app}=A.B	Error = Exact Approx
0	0	0	0	0	0	0
0	1	1	0	1	0	0
1	0	1	0	1	0	0
1	1	0	1	1	1	-1

A.Proposed 4-Bit Approximate Vedic Multiplier The architecture of AVMT, is designed by utilizing the principles of the AVM2 in a cascaded manner, is shown in Fig.3. This multiplier operation is described in two stages. In the first stage, the 4-bit numbers are divided into two sets of 2bit numbers, and each set is multiplied using the AVM2

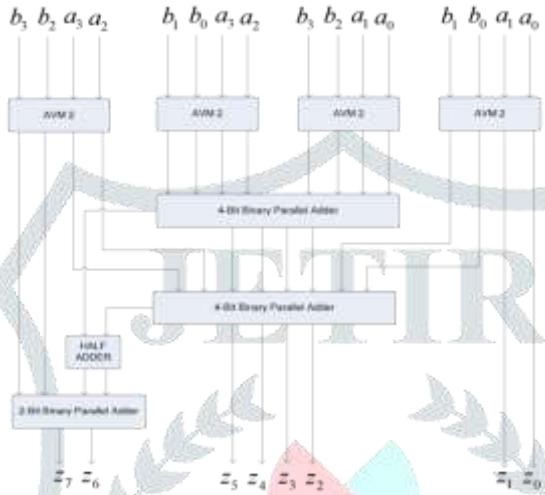

Fig.3. 4-bit Approximate Vedic Multiplier

The results from the first stage are partial products. In the second stage, Binary parallel adders are used to add partial products to obtain the final 8-bit product Z7…Z0. This architecture takes advantage of the UrdhvaTiryakbhyam method's simplicity and effectiveness with approximate computing. It's noteworthy that 8 XOR gates have been replaced with 8 OR gates in this design, and this is due to the use of AVM2.

III. RESULT ANALYSIS AND DISCUSSION

AVMT and other conventional multipliers are coded in Verilog and synthesized using Xilinx ISI 14.7. RTL diagram and functional verification of the proposed AVMT circuit are shown in Fig. 4 and Fig. 5 respectively. The simulation result is shown in Table 2.

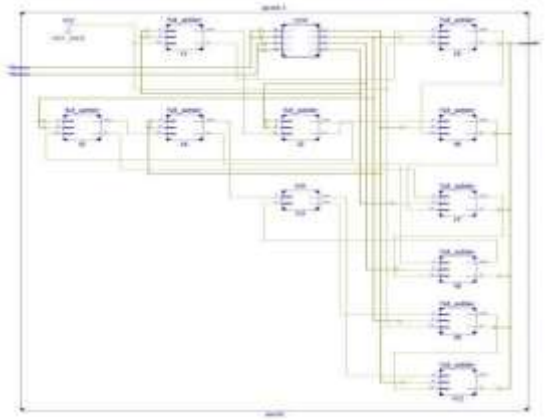

Fig.4. RTL diagram of AVMT

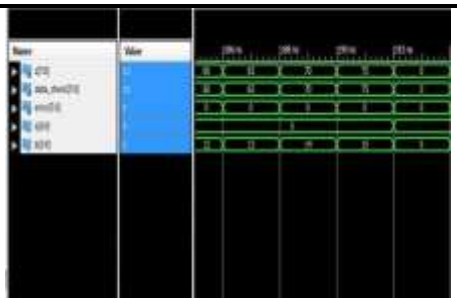

Fig.5. Functional verification of AVMT

TABLE. 2. COMPARING AVMT WITH VARIOUS MULTIPLIERS

Multipliers	LUT	Delay
Exact Vedic Multiplier	54	4.12 ns
Array Multiplier	50	3.97ns
AVMT(Proposed)	48	3.61 ns

Fig. 6 and 7 illustrate a comparison between AVMT and other multipliers for various parameters. AVMT shows high speed and lower area compared to the exact Vedic multiplier and array multiplier.

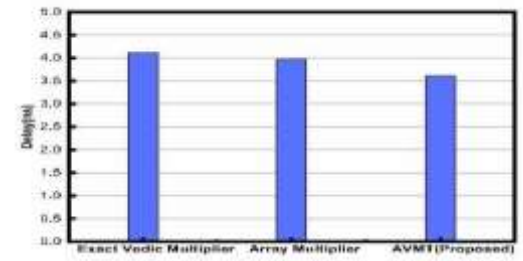

Fig.6. Comparision of different multiplier for Delay(ns)

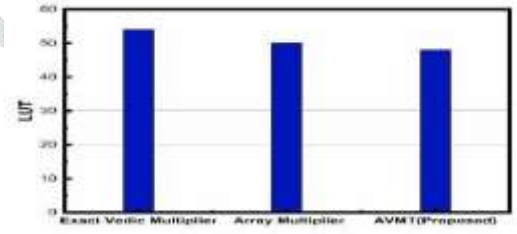

Fig.7. Comparison of different multiplier for LUT

The proposed architecture achieves an 11% less area and a 12% increase in processing speed compared to the exact Vedic multiplier. In this design, eight XOR gates have been replaced with 8 OR gates. Compared to OR gates, XOR gates often use more power, take up more area, and can cause slower signal propagation. As a result, at the cost of accuracy, the proposed AVMT circuit is more energy efficient than the others. For accuracy analysis, AVMT is coded into MATLAB and apply all possible inputs. For 256 inputs, only 49 output is erroneous therefore error rate is 18% which is acceptable for error-resilient applications [12].

IV. APPLICATION BLENDING

Image blending is to be used to check the performance of AVMT. SSIM value is used to check the quality of blended images. The range of SSIM is 0-1.[13] Different test images are taken from [14] and multiplied. SSIM values of different blended images are shown in Table.3 and the average

SSIM value is 0.91 which is high and acceptable value for error resident systems [15-16]. Some Blended images results are shown in Fig.7.

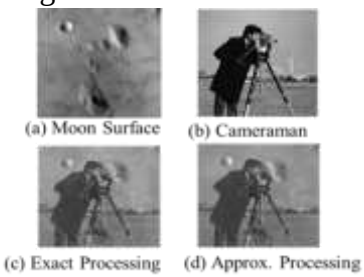

Fig.7. Blending Images using (c) exact multiplier and (d) approximate multiplier

TABLE.3 SSIM VALUE OF MULTIPLIED IMAGES

Image Multiplications	SSIM	Average SSIM
Moon Surface -Cameraman	0.90	0.91
Gray- Camerman	0.93	
Car- Cameraman	0.91	
Moon Surface-Clock	0.88	

V. CONCLUSION

In conclusion, this research has demonstrated the potential of approximate computing, specifically in the context of a 4-bit approximate Vedic multiplier, as a viable solution for energy efficient computing. By striking a careful balance between computational accuracy and performance gains, the proposed AVMT showcases notable advantages over conventional multipliers. AVMT has an 11% reduction in area and a 12% increase in processing speed compared to the exact Vedic multiplier. Moreover, the use of AVMT in image blending applications highlights its practicality in real-world scenarios. The obtained SSIM value of 0.91 attests to the suitability of the proposed multiplier for demanding image processing tasks, proving that the obtained AVMT system is suitable for error flexible applications.

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