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Design of High Performance 8-bit Vedic Multiplier

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Abstract : Multiplier is an essential Functional Block of the Microprocessor as it is used repeatedly in scientific calculations. Thus the design of fast and low-power binary multipliers are very important, particularly for Digital Siganl Processing. This Project describes the design of fast and low-power 8-bit Multiplier architecture which implements Urdhva-Tiryakbyham sutra of Vedic multiplication. Urdhava means vertical multiplication and Tiryakbyham means crosswise multiplication. This Vedic multiplier uses adders as its fundamental building blocks. these adders are created using Verilog HDL. The design is implemented using Verilog HDL and Xilinx ISE for synthesis and implementation. The Project aims to explore the benefits of Vedic multiplication in terms of speed.

Index terms-VHDL, Urdhva, Tiryakbyham

I. INTRODUCTION

Multiplication is still a crucial arithmetic operation in real-time digital signal processing (DSP) applications, where the exponential rise of technology has accelerated the requirement for speed and efficiency. Many multiplier designs have been created throughout the years to address this, all to increase speed and efficiency. Of them, Vedic multipliers have been a prominent option because of their lower power consumption and higher speed in comparison to conventional array and Booth multipliers. Vedic multipliers have their roots in ancient Indian mathematics and use sixteen sutras, or methods. One particularly useful sutra for quick and efficient logical operations is the Urdhava Tiryakbhyam sutra.

The rapid advancement of technology has fueled the demand for fast and efficient real-time digital signal processing applications, where multiplication stands as a fundamental arithmetic operation. In response, numerous multiplier designs have emerged over the years to improve speed and efficiency. Among these, Vedic Multipliers have gained prominence for their exceptional speed and low power consumption compared to traditional array and Booth Multipliers. Utilizing sixteen sutras or algorithms, Vedic Multipliers, particularly those employing the Urdhava Tiryakbhyam sutra, excel in logical operations, offering unparalleled efficiency in terms of speed. This paper aims to explore the wide-ranging applications of Vedic Multipliers in the domains of image processing and digital signal processing. Specifically, it focuses on various modifications of existing Vedic Multiplier architectures aimed at enhancing their speed and performance parameters.

In recent years, the demand for real-time processing capabilities has surged across a multitude of applications, spanning from multimedia systems to wireless communications and medical imaging. Within these applications, the ability to execute complex mathematical operations with minimal latency is crucial for ensuring smooth operation and optimal performance. Multiplication, being a fundamental operation in many signal processing algorithms, has been a focal point for optimization efforts. Traditional multiplier designs, such as Array, Wallance tree and Booth multipliers, have served their purpose well but are often limited in terms of speed and power efficiency, particularly as processing demands continue to escalate. The emergence of Vedic Multipliers represents a significant breakthrough in addressing these limitations. By drawing inspiration from ancient Indian mathematical principles, Vedic Multipliers offer novel approaches to multiplication that significantly enhance speed and efficiency while minimizing power consumption. The Urdhava-Tiryakbhyam sutra, in particular, has been instrumental in achieving remarkable performance gains, making Vedic Multipliers a preferred choice in many high-performance computing applications.

Multipliers play a pivotal role in numerous applications, with Digital signal processing (DSP) standing out as a prime example where the speed of multiplication and considerations regarding area and power consumption are paramount. In Digital signal processing (DSP) tasks such as filtering, Fourier transforms, and Convolution, the efficient execution of multiplication operations directly impacts the overall performance and responsiveness of the system. The objective of developing optimal multipliers lies in striking a delicate balance between power consumption and speed. Low power consumption is essential for prolonging battery life in portable devices, minimizing heat dissipation in high-density computing environments, and reducing overall energy costs in large-scale deployments. Conversely, high-speed multiplication is crucial for meeting real-time processing requirements, ensuring timely responses in critical applications such as audio processing, communications, and medical imaging. It's imperative to select an appropriately optimized multiplier design, as the choice directly influences the

overall performance and efficiency of digital circuits. Failure to do so can lead to tailback, delays, and inefficiencies, ultimately hampering the functionality and responsiveness of digital systems. Therefore, the quest for optimal multipliers remains a central focus in the ongoing advancement of digital circuit design and implementation, driving innovations that enable faster, more efficient, and more reliable computing solutions across a diverse range of industries and applications.

II. LITERATURE

Multipliers are fundamental components in microprocessors, essential for a variety of scientific and engineering computations. Their importance is particularly pronounced in Digital Signal Processors (DSPs), where multiplication operations are frequently executed in tasks such as filtering, Fast Fourier Transforms (FFT), and Discrete Fourier Transforms (DFT). The efficiency of these multipliers directly impacts the overall performance and power consumption of DSP systems. Consequently, the development of fast and low-power multipliers has been a focal point of research.

Array multipliers, also known as parallel multipliers, are known for their speed as they generate all partial products simultaneously using AND gates. The final product is obtained by adding these partial products using a network of adders. Despite their speed advantages, the performance of array multipliers is significantly influenced by the propagation delay of the full adders and half adders used in summing the partial products. This delay also affects power consumption, making efficient design crucial for high-performance applications.

Booth multiplication algorithm is another widely used method, particularly advantageous for smaller operand sizes. It reduces the number of required addition operations by encoding the multiplicand based on the bits of the multiplier, effectively speeding up the multiplication process. However, Booth multipliers become less efficient with larger operand sizes, limiting their application in high-speed multiplications required in advanced DSP tasks.

Wallace and Dadda tree architectures have been proposed. These methods focus on minimizing the number of sequential adding stages by employing a hierarchical reduction of partial products, significantly reducing the propagation delay. Wallace tree multipliers, in particular, are known for their speed but suffer from highly irregular structures, which complicates their implementation and increases the required silicon area.

III. VEDIC MULTIPLIER

Vedic mathematics, derived from ancient Indian scriptures, offers a set of algorithms known as sutras that simplify complex arithmetic operations. Among these, the Urdhva-Tiryakbhyam (Vertically and Crosswise) sutra is highly efficient for multiplication. This method generates partial products in parallel and sums them simultaneously, similar to array multipliers but with improved speed and reduced complexity.

Vedic multipliers have gained attention for their compact design and efficiency. The Urdhva-Tiryakbhyam sutra, in particular, facilitates a high-speed multiplication process with minimal propagation delay, resulting in low power consumption and reduced silicon area. These attributes make Vedic multipliers suitable for real-time DSP applications and small-scale wireless sensor networks where both speed and power efficiency are critical.

The 8-bit Vedic Multiplier is an architecture that combines ancient Vedic multiplication principles with modern computing techniques to efficiently handle 8-bit operands. It leverages methodologies like vertical and crosswise multiplication to streamline computation while ensuring precision and efficiency. Fundamental components such as adders are optimized to support Vedic principles, enabling fast and accurate multiplication operations. Efficiency and performance are prioritized, with a focus on minimizing computation time and resource utilization. Implementation is facilitated through hardware description languages like Verilog or VHDL, with synthesis tools aiding in optimization and verification. Overall, the 8-bit Vedic multiplier represents a powerful tool for digital arithmetic, offering speed, precision, and versatility in numerical computations.

IV. PROPOSED MODEL

The 8x8 Vedic Multiplier is an advanced architecture designed for efficient multiplication operations with 8-bit operands, incorporating principles from Vedic mathematics. It streamlines the multiplication process by leveraging Vedic techniques like vertical and crosswise multiplication. Key components include eight 8-bit operands, partial product generation units, and an accumulation unit. This architecture optimizes performance and resource utilization, offering faster computation speeds and reduced hardware complexity compared to conventional methods. Implementation is facilitated through hardware description languages like Verilog or VHDL, with synthesis tools aiding in optimization and verification. Overall, the 8x8 Vedic Multiplier provides an efficient solution for large-scale multiplication tasks in digital systems.

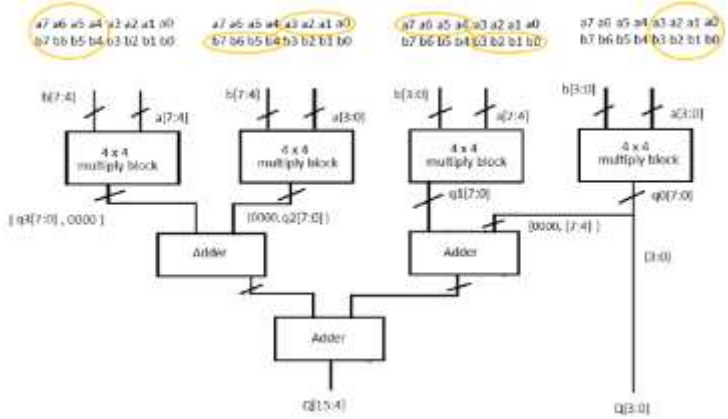

Fig.1. Block diagram of 8x8 Vedic Multiplier

The flow chart begins by accepting two 8-bit binary numbers as input, which are subsequently divided into two 4-bit halves each. These halves are then used to perform four 4-bit multiplications, generating partial products. Specifically, the lower 4 bits of each number are multiplied, followed by the cross-multiplications of the higher and lower 4-bit segments, and finally the multiplication of the higher 4 bits of both numbers. These partial products are then appropriately shifted to their respective positions and summed to produce the final 16-bit result. By breaking down the process into these smaller, manageable steps and visually representing them, the flow chart elucidates the efficient and systematic approach of the Vedic multiplication technique, ensuring clarity and ease of implementation. The below figure shows the flow chart of 8 bit Vedic Multiplier.

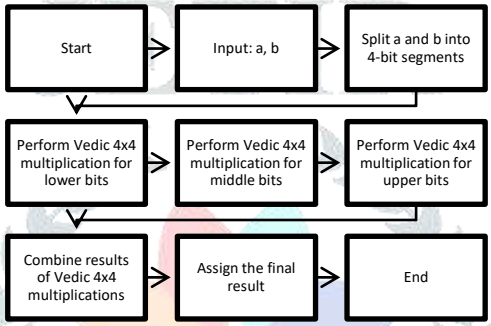

Fig 2: Flow Chart for 8x8 Vedic Multiplication

V. RESULT

The 8-bit Vedic multiplier was designed and synthesized using Xilinx tools, aiming to optimize performance in terms of delay and power consumption. The design utilizes 140 Look-Up Tables (LUTs) and 32 Input/Output (I/O) pins, demonstrating efficient resource utilization. Below is a detailed summary of the results obtained from the synthesis and simulation processes.

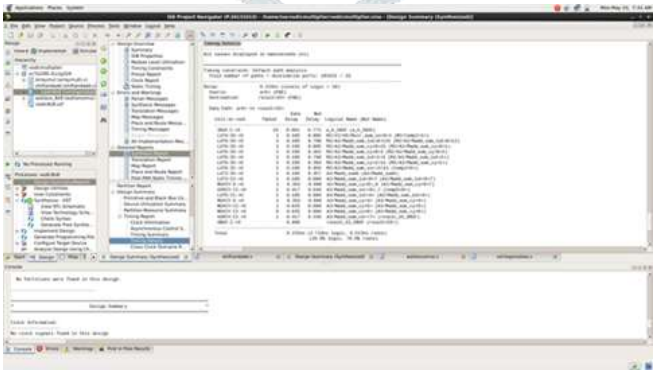

Fig 3: Critical path Window of 8-bit Vedic Multiplier

The 8-bit Vedic multiplier demonstrates a clear advantage in terms of delay, making it a superior choice for applications requiring high-speed arithmetic operations. Its innovative approach, derived from Vedic mathematics, ensures fewer computational steps and reduced delay, outperforming the Array, Wallace Tree, and Shift-and-Add multipliers. This makes the Vedic multiplier an excellent choice for inclusion in high-performance digital systems where speed is a critical factor.

Table1: Comparision of Delays of Vedic Multiplier with Other Multipliers

S.no	Name of the Multiplier	Delay(ns)
1.	8-bit Vedic Multiplier	9.232ns
2.	8-bit Array Multiplier	13.900ns
3.	8-bit Shift-and-Add Multiplier	12.163ns
4.	8-bit Wallace Tree Multiplier	11.591ns

VI. CONCLUSION

The 8x8 Vedic Multiplier stands out as a promising solution in digital arithmetic, offering significant improvements in computational efficiency and reduced delay by leveraging the Urdhva Tiryakbhyam sutra. Its application spans various computing domains, including DSP, FPGAs, and ASICs, enhancing performance in traditional systems and emerging technologies. Future research can explore scaling to larger bit-widths, optimizing for low-power applications, developing parallel and pipelined architectures, and integrating error detection and correction mechanisms. Additionally, adapting Vedic principles to quantum computing, creating educational tools, and applying Vedic multiplication in AI and machine learning accelerators are promising directions. These avenues can unlock the full potential of the 8x8 Vedic Multiplier, driving advancements in digital arithmetic and computing technologies.

VII. REFERENCES

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